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Feb. 26, 1987 NAME BENMEI CHEN

(1) (30 pts) Given the iterative equations:

$$f(i,j) = f(i,j-1) \text{ OP } g(i-1,j)$$
$$g(i,j) = g(i-1,j) \text{ OP } f(i,j-1) \quad \text{for } i,j = 1,2,3$$

where OP is a specific operator. (a) Expand this computation totally into the space domain. (b) Expand this computation totally into the time domain. (c) Assume the time delay associated with OP is T, design a 1D pipeline for this equation. What is the clock period of the pipeline? (Assume the latch time delay is negligible).

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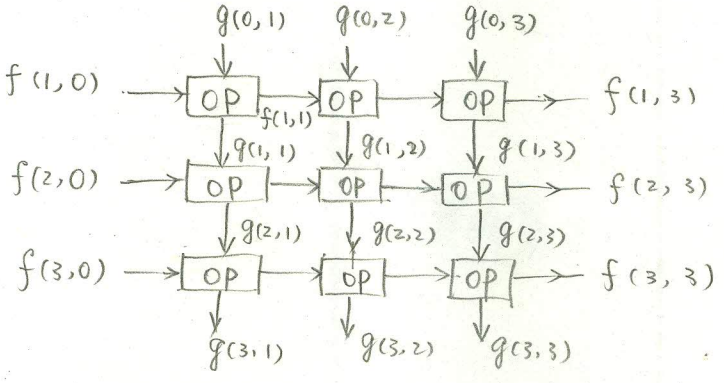
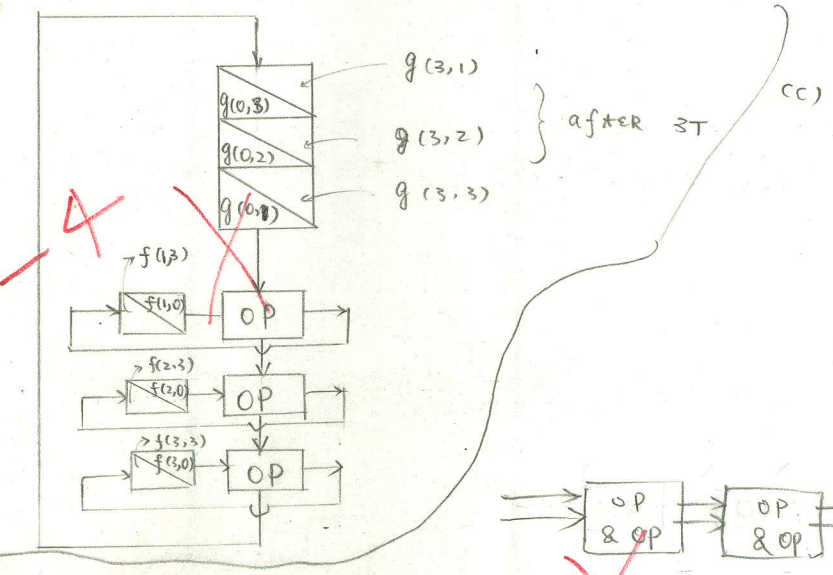
SOLUTION:

(a) Expand into the space domain.



(b) Expand into the time domain



(c)

(c) the clock period = 2T

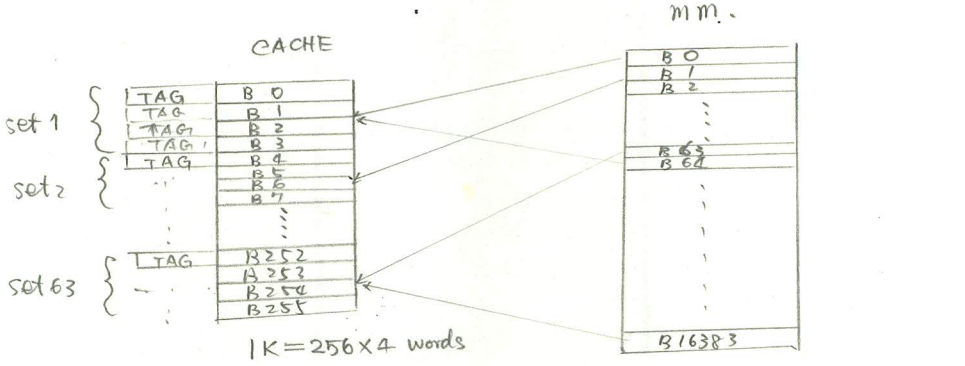
1D PIPELINE

-4

-8

3T?

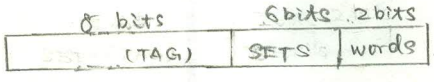
(2) (20 pts) A uniprocessor has 1K cache memory and 64K RAM main memory. Assume the set associative address mapping is used in this system. The memory is divided into blocks of 4 words, and there are 4 block frames for each set in the cache. (a) Define the bits associated with each field for the physical address. (b) Given a physical address, describe the acess procedure step by step for a cache hit situation. (c) Which set in the cache is the possible location for the binary HEX addresses 3785 and AA92.



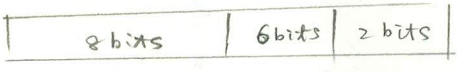
1K = 256 × 4 words
= 256 Blocks
= 64 sets

64K words = 16384 Blocks

(a)



(b)



If we have the address above.

we use the middle 6 bits to dermine the set

and then use the high-order 8-bit to tag the block if the block is occupied. And use the low-order 2bits to select the word.

(c) FOR ADDR, 3785 (H) = 14213 (10) is in block 3553

will go to set 55

FOR AA92 (16) = 43666 (10) is in block 10916

will go to set 42.

(3) (20 pts) Given an interleaved main memory with 8 memory modules. Each module has 2K words. (a) Show the address format for this system, and the distribution of addresses into memory modules. (b) What is the maximun bandwith when access consecutive words? (c) What is the maximum bandwidth when one module fails? (assuming all the modules can be access at the same time)

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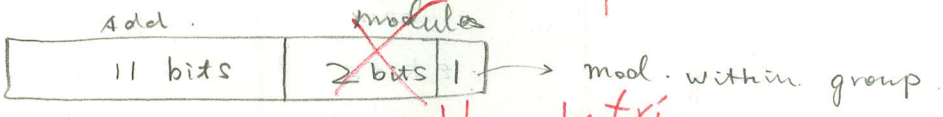
(a) Give high-order interleaved main memory

-1



addr. distri. -2

(b) Assume the memory access time is Ta.

maximum bandwitth = $8/Ta$. Because the maximum average rate per word is $Ta/M = Ta/8$

-5

(c)

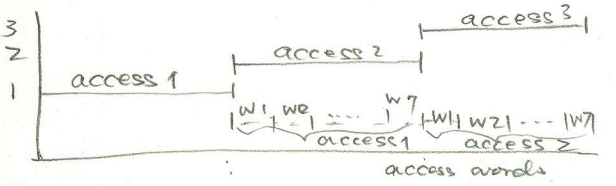
max. bandwidth = $4/Ta$.

From the address format above if we have module fail. we can only use 2 bits as the module addresses. So, only 4 moudules cane be used with some tech.

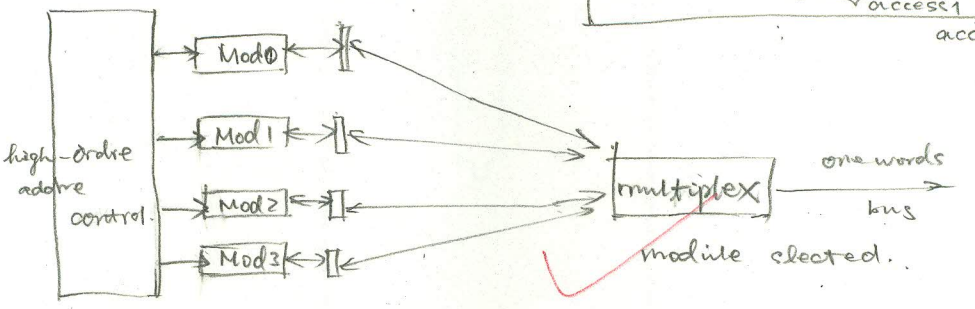
-3

(4) (30 pts) Given an interleaved memory with 4 memory modules. Each module has 2K words. (a) Show the block diagram for S_access configuration. Describe the memory access procedure step by step. (b) Do part (a) for C_access. (c) Do part (a) for C/S access. Assuming there are two memory banks with two modules each.

-8

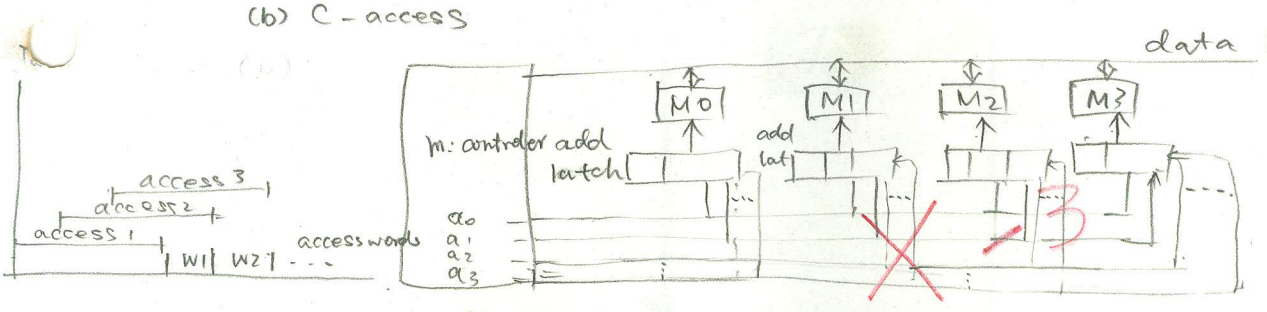


(a) S-access



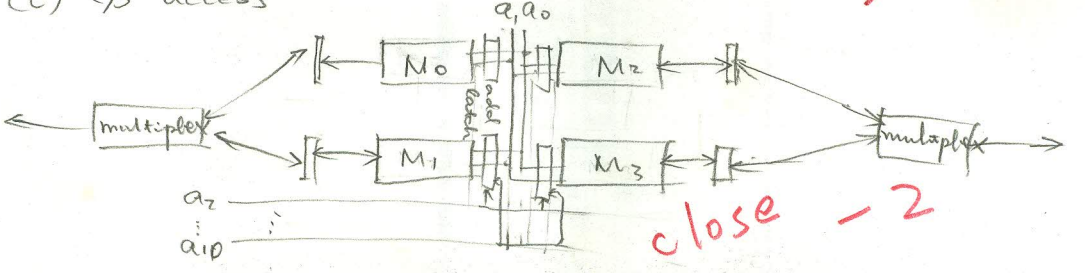
When the memory do accessing, all the modules access simultaneously to the latches and then multiplex select the word.

(b) C-access



Address put in addr. latch. then adjust the access distance, we can have different sequential of data

(c) C/S access



close -2

We have 2 different accesses to blocks of 2 modules at the same time

description -2

EE 524 EXAM #2 (76) Name BENMEI CHEN

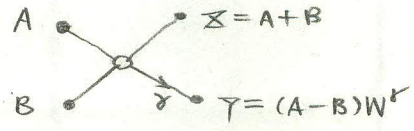
April 14, 1987

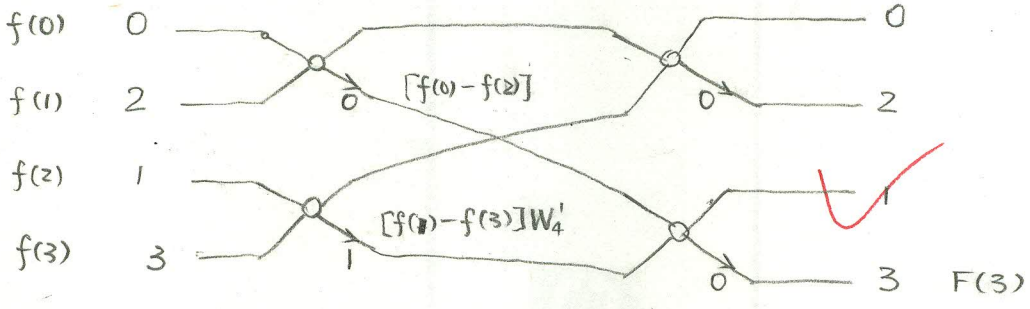
(20 points)

1. (A) Use butterfly operator to express a 4-point FFT operation.

(B) Assume the input points are f(0), f(1), f(2), and f(3). What is the expression for the Fourier point F(3)?

(A) THE BUTTERFLY OPERATOR IS DEFINED AS





(B) $$F(3) = \frac{1}{2}\left\{\frac{1}{2}[f(0)-f(2)] - \frac{1}{2}[f(1)-f(3)]W_4^1\right\}$$

$$= \frac{1}{4}\left\{f(0) - f(2) + f(1)W_4^1 - f(3)W_4^1\right\}$$

$$= \frac{1}{4}\left\{f(0) - f(1)W_4^1 + f(2)W_4^2 - f(3)W_4^3\right\}$$

(30 points)

2. (A) Given the reservation table for task A, find out its collision vector, minimum average latency (MAL), and the lower bound of MAL.

(B) Use elemental delay unit to change the given reservation table, so the MAL reaches its lower bound. If the cycle C is the cylce which produces the lower bound MAL, then what is the set of all possible time intervals between initiations derived from cycle C with period equals 8.

Task A:

	0	1	2	3	4
S_0	X		X		
S_1		X			X
S_2				X	X

(A) $F = \{1, 2, 3\}$

THE collision vector $C = (0\,1\,1\,1)$ ✓

MAL = 4 ✓

$G_c = (0, 4, 8, 12 \cdots)$

$\bar{G}_c = (1, 2, 3, 5, 6 \cdots)$

$\bar{G}_c \pmod 4 = (1, 2, 3)$

The lower bound of MAL = ~~8/3~~ $= 2.667$ -3

(B)

S_0	X		X					
S_1		X			d	d	d	X
S_2				X	d	X		

o.k.

G_c.? -2

3. Assume a parallel computer system has N processing elements (PE) connected via a perfect shuffle network. Each PE has a $n = \log_2 N$ bit address.

-1

(7 pts) (A) Use the binary address show the effect of shuffle.

(8 pts) (B) If N equals 8, what is the permutation function caused by endless shuffle operation.

(15 pts) (C) Show by example that an 4 x 4 matrix can be transposed in two perfect shuffles when it is stored as a 1D vector of length 16 in 16 processors.

(A) Assume the binary address of the PEs is $a_{n-1}a_{n-2}\cdots a_1 a_0$

$$S(a_{n-1}a_{n-2}\cdots a_1 a_0) = a_{n-2}\cdots a_1 a_0 a_{n-1}$$ ✓

(B) $8\times 7\times 6\times\cdots\times 2\times 1 = 8!$

X -4

(C)

	S/E
0000	0000 / 0001
0001	1000 / 1001
0010	0001 / 0000
0011	1001 / 1000
0100	0010 / 0011
0101	1010 / 1011
0110	0011 / 0010
0111	1011 / 1010
1000	0100 / 0101
1001	1100 / 1101
1010	0101 / 0100
1011	1101 / 1100
1100	0110 / 0111
1101	1110 / 1111
1110	0111 / 0110
1111	1111 / 1110

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4. In Cray-1 every operand has to be stored in either scalar register or vector register in order to catch up with the speed of arithmetic pipelines. Show the internal operations, in register transfer level, of Cray-1 for the following DO loop. Clearly indicate where the chaining operation is possible

```
DO 10 I = 1, 30

10 A(I) = 5.0*B(I) + C
```

where A and B are vectors of length 30. C is a constant. All the variables are stored in the memory.

The internal operations:

FIRST

$S_2 \leftarrow 5.0$

$V0 \leftarrow$ memory (B)

$S_1 \leftarrow$ mem. C

Chain Op.

$V0 \leftarrow$ memory (B)

$V1 \leftarrow S_2 \times B$

$V2 \leftarrow V1 + S_1$

Memory $\leftarrow V2$