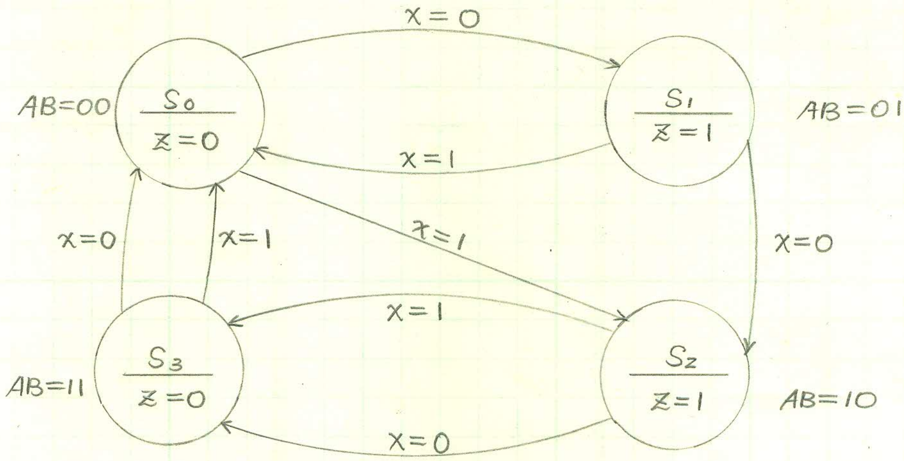
GIVEN THE STATE GRAPH,



(1) DESIGN A CIRCUIT USING J-K FLIP-FLOPS.

(2) DRAW A TIMING CHART SHOWING X, J_A, K_A, J_B, K_B, Q_A, Q_B, Z, CLOCK.

FOR INPUT SEQUENCE $X = 0100111$.

SOLUTION: SINCE THERE ARE 4 STATES IN THE STATE GRAPH, WE HAVE TO USE 2 J-K FLIP-FLOPS IN THE CIRCUIT. THAT IS J-K FF A AND J-K FF B. LET $S_0 \sim AB=00$, $S_1 \sim AB=01$, $S_2 \sim AB=10$ AND $S_3 \sim AB=11$. SO, WE HAVE THE STATE TABLE FOR THE SYSTEM.

TABLE 13-6, ON P278

J-K FLIP-FLOP

Q	Q^+	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

$Q^+ = JQ' + K'Q$

X	A	B	A^+	B^+	J_A	K_A	J_B	K_B	Z
0	0	0	0	1	0	x	1	x	1
0	0	1	1	0	1	x	x	1	1
0	1	0	1	1	x	0	1	x	0
0	1	1	0	0	x	1	x	1	0
1	0	0	1	0	1	x	0	x	1
1	0	1	0	0	0	x	x	1	0
1	1	0	1	1	x	0	1	x	1
1	1	1	0	0	x	1	x	1	0

FOLLOWING ARE J-K FLIP-FLOP INPUT EQUATIONS:

J_A

AB \ X	0	1
00	0	1
01	1	0
11	x	x
10	x	x

K_A

AB \ X	0	1
00	x	x
01	x	x
11	1	1
10	0	0

J_B

AB \ X	0	1
00	1	0
01	x	x
11	x	x
10	1	1

K_B

AB \ X	0	1
00	x	x
01	1	1
11	1	1
10	x	x

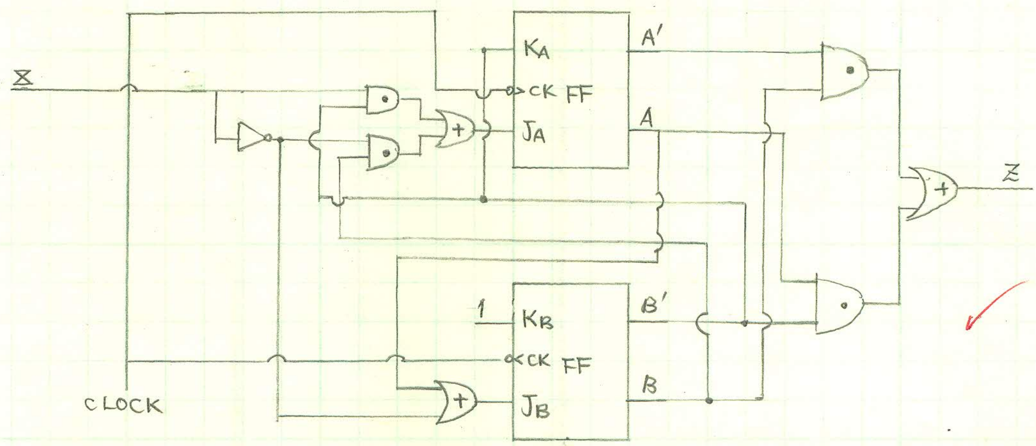
Z

B^+ \ A^+	0	1
0	0	1
1	1	0

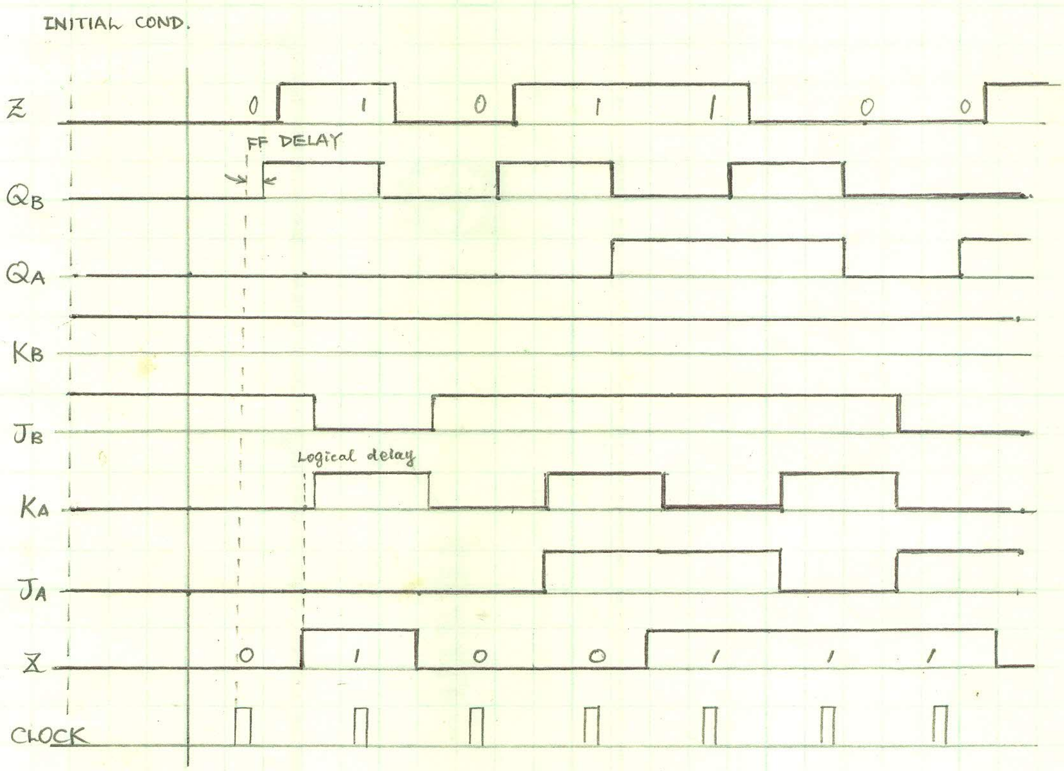
$J_A = X'B + XB'$ ✓ $K_A = B$ ✓ $J_B = X' + A$ ✓ $K_B = 1$ ✓ $Z = (A^+)'B^+ + A^+(B^+)'$ ✓

HOMEWORK NO: 1 | Fundamentrals of System | BENMEI CHEN

(1) The circuit:



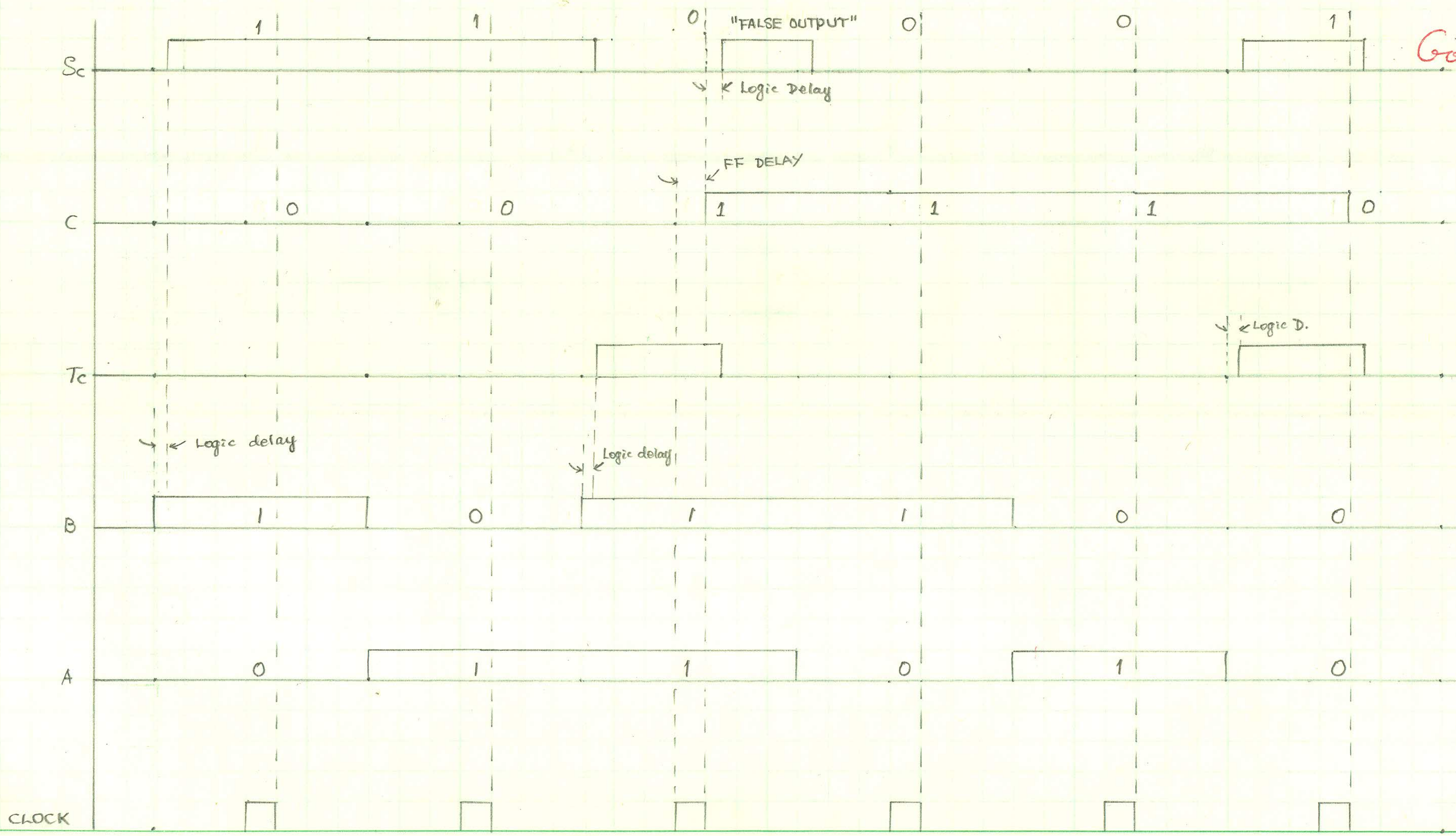
(2) THE TIMING CHART:



Draw the timing chart for the example in the lecture 2 (Mealy - adder network):

$$T_c = AB\bar{C} + \bar{A}\bar{B}C \quad , \quad S_c = A \oplus B \oplus C \quad , \quad \text{FOR} \quad A = 010110 \; , \; B = 001101$$

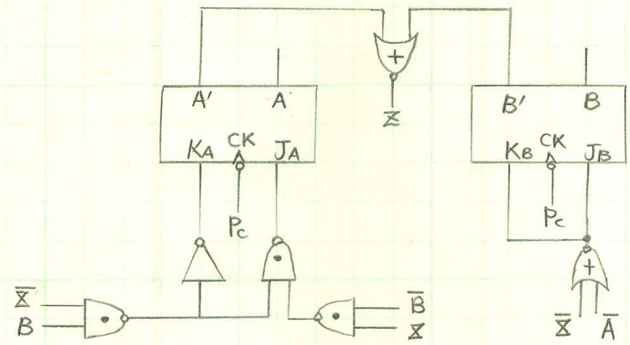
Solution: We used to add two numbers from low-level to high-level, SO, the input A and B have to be A=011010, B=101100.



Good

10

14.3 (a) For the following sequential network, find the next state equation or map for each flip-flop. Using these next state equations or maps construct a (Moore) state table and graph for the network.



SOLUTION:

$$J_A = \overline{(\overline{X\bar B})\cdot(\overline{\bar X \cdot B})} = (X\bar B) + (\bar X \cdot B)$$

$$K_A = \overline{(\overline{\bar X \cdot B})} = \bar X B$$

$$J_B = \overline{(\bar X + \bar A)} = XA$$

$$K_B = J_B = XA$$

$$Z = \overline{(\bar A + \bar B)} = AB$$

The next state equations:

$$A^+ = J_A \bar A + \bar K_A A = (X\bar B + \bar X B)\cdot \bar A + (X + \bar B)A$$

$$= \bar A \bar B X + \bar A B \bar X + AX + A\bar B$$

$$B^+ = J_B \bar B + \bar K_B B = XA\bar B + (\bar X + \bar A)B = A\bar B X + \bar A B + B\bar X$$

OR, the next state map:

A^+

AB \ X	0	1
00	0	1
01	1	0
11	0	1
10	1	1

B^+

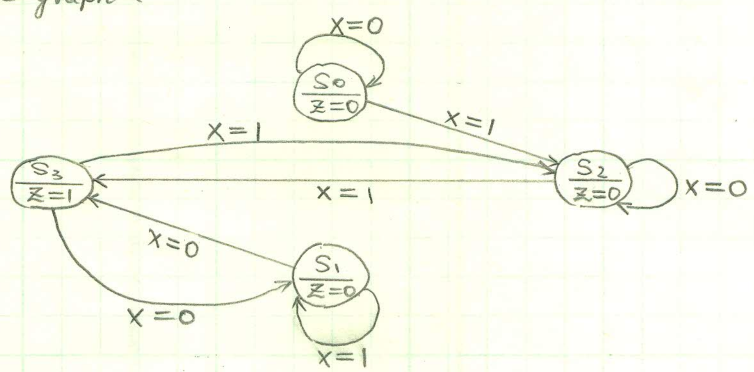
AB \ X	0	1
00	0	0
01	1	1
11	1	0
10	0	1

The Moore state table for the network: (Let $S_0: AB=00$, $S_1: AB=01$, $S_2: AB=10$, $S_3: AB=11$)

	A	B	A^+B^+ $X=0$	A^+B^+ $X=1$	Z
S_0	0	0	0 0	1 0	0
S_1	0	1	1 1	0 1	0
S_2	1	0	1 0	1 1	0
S_3	1	1	0 1	1 0	1

Present state	$X=0$ next state	$X=1$ next state	Z
S_0	S_0	S_2	0
S_1	S_3	S_1	0
S_2	S_2	S_3	0
S_3	S_1	S_2	1

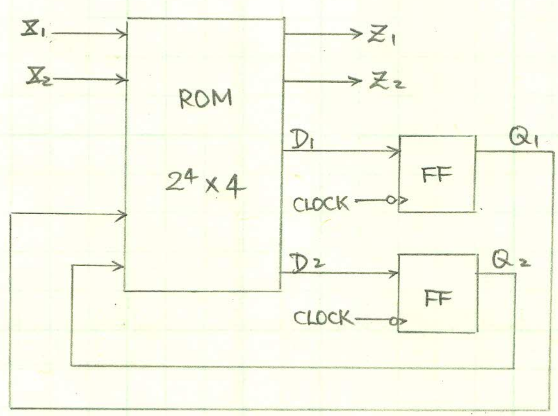
The Moore state graph:



14.9 A sequential network is constructed using a ROM and two D flip-flops as shown below. The contents of the ROM is given in the table.

a. Draw a timing diagram for the network for the input sequence $X_1X_2 = 10, 01, 11, 10$, Assume that input changes occur midway between clock impluses. Indicate any false outputs on the diagram, and specify the correct output sequence for Z_1 and Z_2.

b. Construct a transition table and state graph for the network.



Q_1	Q_2	X_1	X_2	D_1	D_2	Z_1	Z_2
0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	0
0	1	0	0	1	1	0	0
0	1	0	1	1	1	1	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	1
1	0	0	0	1	1	0	0
1	0	0	1	0	0	0	0
1	0	1	0	1	1	0	1
1	0	1	1	0	0	0	1
1	1	0	0	1	0	0	0
1	1	0	1	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	1	0	1	0	0

SOLUTION: (a) From the table shown above, we are able to have

D_1

X_1X_2 \ Q_1Q_2	00	01	11	10
00	0	1	1	1
01	0	1	0	0
11	0	1	0	0
10	0	1	1	1

D_2

X_1X_2 \ Q_1Q_2	00	01	11	10
00	0	1	0	1
01	0	1	1	0
11	1	0	1	0
10	1	0	0	1

Z_1

X_1X_2 \ Q_1Q_2	00	01	11	10
00	1	0	0	0
01	1	1	0	0
11	1	1	0	0
10	1	0	0	0

Z_2

X_1X_2 \ Q_1Q_2	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	0	1
10	0	1	0	1

From the tables above, we can write down,

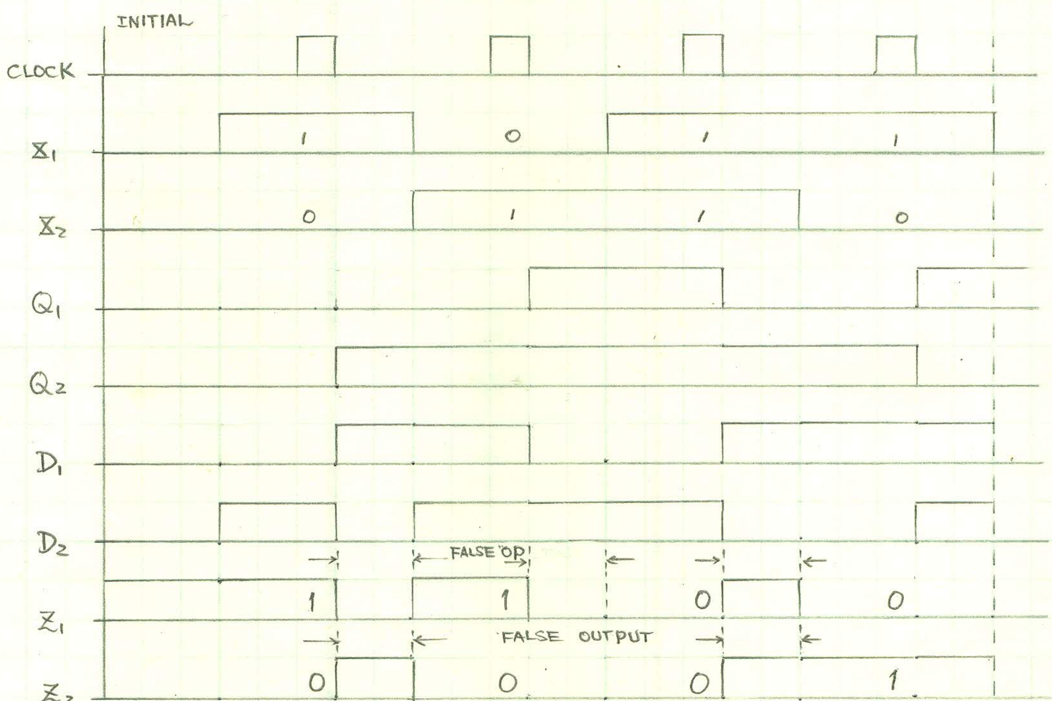
$$D_1 = \bar{Q}_1 Q_2 + \bar{Q}_1 \bar{X}_2$$

$$D_2 = X_1 \bar{Q}_1 \bar{Q}_2 + \bar{X}_1 \bar{Q}_1 Q_2 + X_2 Q_1 Q_2 + \bar{X}_2 Q_1 \bar{Q}_2$$

$$Z_1 = \bar{Q}_1 \bar{Q}_2 + X_2 \bar{Q}_1 Q_2$$

$$Z_2 = X_1 \bar{Q}_1 Q_2 + X_1 Q_1 \bar{Q}_2$$

Now for the input sequence $X_1X_2 = 10, 01, 11, 10$. And assume the initial conditions $Q_1Q_2 = 00$. The following is the timing diagram:



Signals are correct at clock times, but it would be best to include logic & F/F delays

The correct output sequence for $Z_1 = 1100$

$Z_2 = 0001$

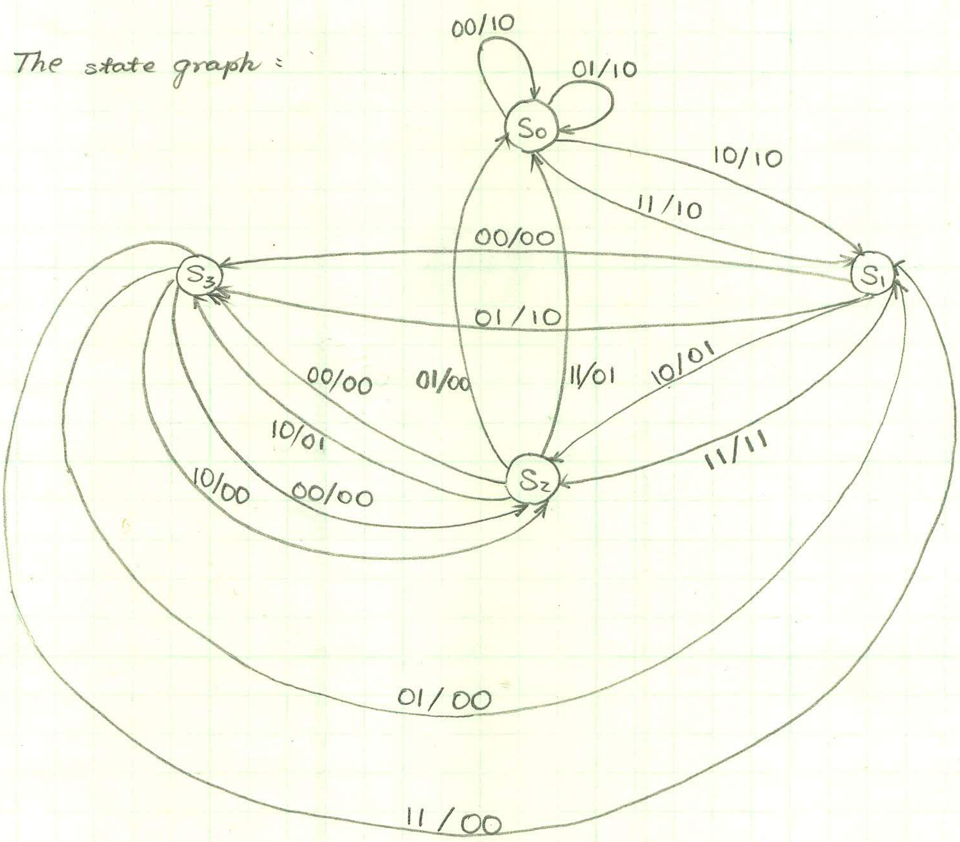
(b)

PRESENT Q_1	Q_2	NEXT $Q_1^+ Q_2^+$ $X_1X_2=00$	01	10	11	PRESENT OUTPUT Z_1Z_2 $X_1X_2=00$	01	10	11
S_0 0	0	0 0	00	01	01	10	10	10	10
S_1 0	1	1 1	11	10	10	00	10	01	11
S_2 1	0	1 1	00	11	00	00	00	01	01
S_3 1	1	1 0	01	10	01	00	00	00	00

OR.

PRESENT STATE	NEXT STATES x=0	1	2	3	PRECENT OUTPUTS Z_1Z_2 x=0	1	2	3
S_0	S_0	S_0	S_1	S_1	10	10	10	10
S_1	S_3	S_3	S_2	S_2	00	10	01	11
S_2	S_3	S_0	S_3	S_0	00	00	01	01
S_3	S_2	S_1	S_2	S_1	00	00	00	00

The state graph :



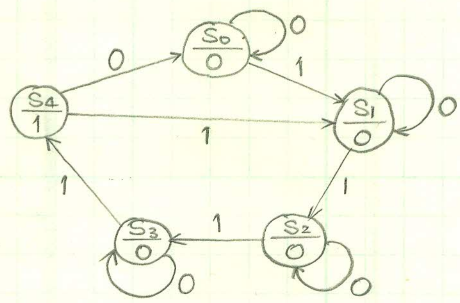
1. Complete the state table 15-4 on page 325, using J-K Flip-flops (T 13-6.)

AB	A^+B^+ X=0	A^+B^+ X=1	Z	X=0 $J_A K_A$	X=0 $J_B K_B$	X=1 $J_A K_A$	X=1 $J_B K_B$
00	00	01	0	0 x	0 x	0 x	1 x
01	11	01	0	1 x	x 0	0 x	x 0
11	00	10	0	x 1	x 1	x 0	x 1
10	11	01	1	x 0	1 x	x 1	1 x

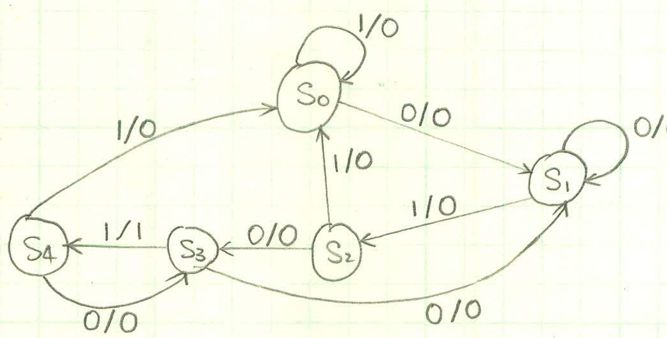
t_a ? t_b

2. Draw stat diagram.

a) Find four ones, output 1 & go to state zero. (Moore)



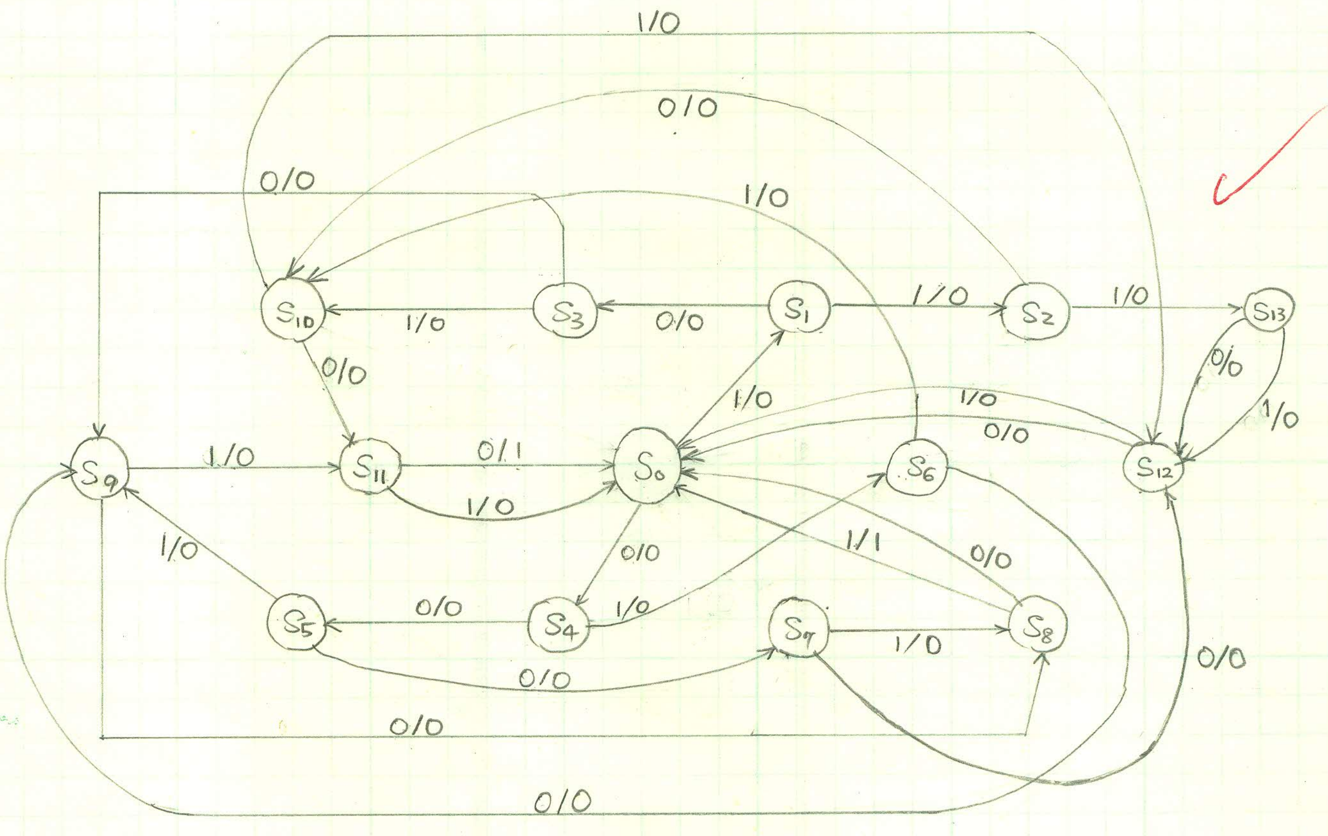
b) Search for sequence 0101, output 1 wherever it occurs (Mealy).



CHECK: X = 0 0 1 1 0 1 1 0 0 1 0 1 0 1 0 0 1 0 1 0 1 1 0

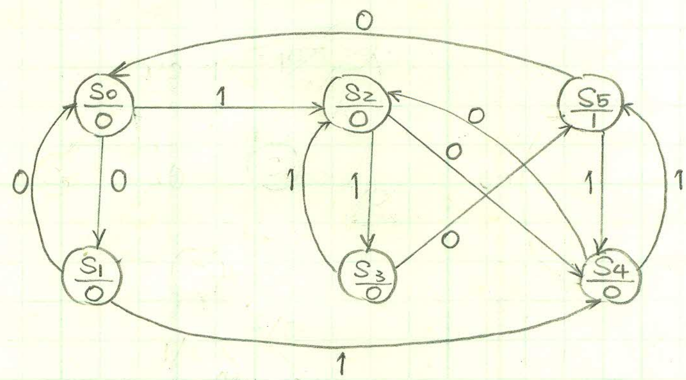
Z = 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 1 0 1 0 0

15.9 The input to a sequential network consists of groups of 5 bits. Each group of 5 bits represents a 2-out-of-5 binary-coded decimal digit (see Table 1-1). After receiving 5 bits, the network should output a 1 and reset if the bit pattern represents a valid 2-out-of-5 BCD digit; otherwise the network should output a 0 and reset. Derive a Mealy state graph (13 states minimum).



CHECK: DECIMAL DIGIT	FROM LOW-LEVEL TO HIGH LEVEL	STATE LOOP
0	11000	$S_0 S_1 S_2 S_{10} S_{11} S_0$
1	10100	$S_0 S_1 S_3 S_{10} S_{11} S_0$
2	01100	$S_0 S_4 S_6 S_{10} S_{11} S_0$
3	10010	$S_0 S_1 S_3 S_9 S_{11} S_0$
4	01010	$S_0 S_4 S_6 S_9 S_{11} S_0$
5	00110	$S_0 S_4 S_5 S_9 S_{11} S_0$
6	10001	$S_0 S_1 S_3 S_9 S_8 S_0$
7	01001	$S_0 S_4 S_6 S_9 S_8 S_0$
8	00101	$S_0 S_4 S_5 S_9 S_8 S_0$
9	00011	$S_0 S_4 S_5 S_7 S_8 S_0$

15.11 A Moore sequential network has one input and one output. The output should be 1 if the total number of 0's received is odd and the total number of 1's received is an even number greater than 0. Derive the state graph and table (6 states).



CHECK : LET $X = 0\ 1\ 0\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 1\ 0\ 0\ 1\ 0\ 1\ 0\ 1$

$Z = 0\ 0\ 0\ 0\ 1\ 0\ 0\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 0\ 0\ 1\ 0\ 0\ 0\ 1$

STATE TABLE

PRESENT STATE	NEXT STATE $X = 0$	$X = 1$	PRESENT OUTPUT
S_0	S_1	S_2	0
S_1	S_0	S_4	0
S_2	S_4	S_3	0
S_3	S_5	S_2	0
S_4	S_2	S_5	0
S_5	S_0	S_4	1

16.2 Reduce the following state table to a minimum number of states.

10

PRESENT STATE	NEXT STATE x=0	NEXT STATE x=1	PRESENT OUTPUT (Z)
a	f	d	0
b	d	a	1
c	h	b	0
d	b	c	1
e	g	b	0
f	a	h	0
g	e	c	0
h	c	f	0

SOLUTION: WE ARE GOING TO REDUCE THE STATES BY USING IMPLICATION CHART. THE FOLLOWING IS THE IMPLICATION CHART FOR TABLE ABOVE.

	a	b	c	d	e	f	g
b	X						
c	f-h d-b	X					
d	X	~~d-b~~ a-c	X				
e	~~f-g~~ ~~d-b~~	X	~~h-g~~ ~~b-b~~	X			
f	~~f-a~~ ~~d-h~~	X	~~h-a~~ ~~b-h~~	X	~~g-a~~ ~~b-h~~		
g	~~f-e~~ ~~d-c~~	X	~~h-e~~ ~~b-c~~	X	~~g-e~~ ~~b-c~~	~~a-e~~ ~~h-c~~	
h	~~f-c~~ ~~d-f~~	X	~~h-c~~ ~~b-f~~	X	~~g-c~~ ~~b-f~~	a-c ~~h-f~~	~~e-c~~ ~~c-f~~

FROM THE IMPLICATION CHART, WE HAVE a=c, b=d, f=h

SO, THE MINIMUM NUMBER STATES' TABLE:

PRESENT STATE	NEXT STATE x=0	NEXT STATE x=1	PRESENT OUTPUT (Z)
a	f	b	0
b	b	a	1
e	g	b	0
f	a	f	0
g	e	a	0

16.3 Digital engineer B. I. Nary has just completed the design of a sequential network which has the following state table:

PRESENT STATE	NEXT STATE $x=0$	NEXT STATE $x=1$	OUTPUT $x=0$	OUTPUT $x=1$
S_0	S_1	S_4	0	0
S_1	S_0	S_5	0	0
S_2	S_3	S_5	0	1
S_3	S_2	S_4	0	1
S_4	S_1	S_2	0	0
S_5	S_0	S_3	0	0
S_6	S_1	S_0	0	0

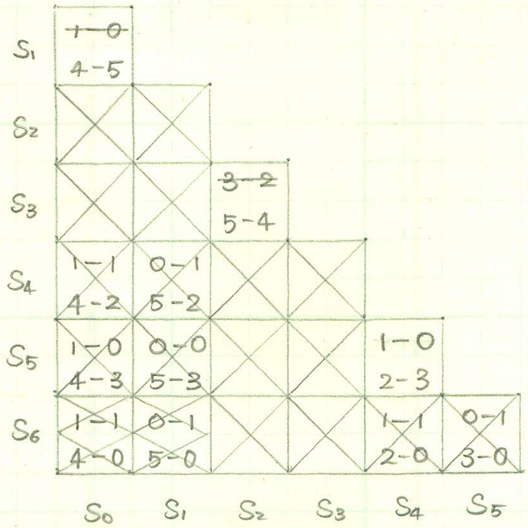
His assistant, F. I. Ipflop, who has just completed this course, claims that his design can be used to replace Mr. Nary's network. Mr. Ipflop's design has the following state table:

	0	1	0	1
σ_0	σ_0	σ_1	0	0
σ_1	σ_0	σ_2	0	0
σ_2	σ_2	σ_1	0	1

a. Is Mr. Ipflop correct?

b. If Mr. Nary's network is always started in state S_0, is Mr. Ipflop correct?

SOLUTION: IN ORDER TO ANSWER THOSE TWO QUESTIONS, WE HAVE TO REDUCE THE STATES IN MR. NARY'S NETWORK. ONCE AGAIN, WE ARE GOING TO USE THE IMPLICATION MOTHED. THE IMPLICATION CHART FOR MR. NARY'S NETWORK IS ON NEXT PAGE.



FROM THE CHART, WE HAVE $S_0 = S_1$, $S_2 = S_3$, $S_4 = S_5$

SO, THE REDUCED STATE TABLE

PRESENT STATE	NEXT STATE x=0	NEXT STATE x=1	OUTPUT x=0	OUTPUT x=1
S_0	S_0	S_4	0	0
S_2	S_2	S_4	0	1
S_4	S_0	S_2	0	0
S_6	S_0	S_0	0	0

NOW, WE ARE ABLE TO ANSWER THOSE QUESTION.

a. O.K. No, because there is no state in Mr. Ipflop's network equivalent to S_6 in reduced Mr. Nary's network.

b. ✓ Yes. If Mr. Nory's network is always started from S_0, then we can never reach S_6 anyway. By replacing S_0 with σ_0, S_4 with σ_1 and S_2 with σ_2, we can get exactly the same network as Mr. Ipflop's (delete the state S_6).

16.1 a. Reduce the following state table to a minimum number of states.

10

PRESENT STATE	NEXT STATE X=0	1	PRESENT OUTPUT 0	1
a	c	f	0	0
b	d	e	-	0
c	h	g	0	0
d	b	g	0	0
e	e	b	0	1
f	f	a	0	1
g	c	g	0	1
h	c	f	0	0

b. You are given two identical sequential networks which realize the above state table. One network is initially in state "a" and the other network is initially in state "c". Specify an input sequence of length three which could be used to distinguish between the two networks, and give the corresponding output sequence from each network.

Solution: So far, we have just studied two methods to reduce the networks to minimum number of states. The first one is called, row matching. And second is the implication table. In this particular problem, we can reduce only one state "a" or "h" by using row matching method. So, we have to use the implication table method to solve this problem.

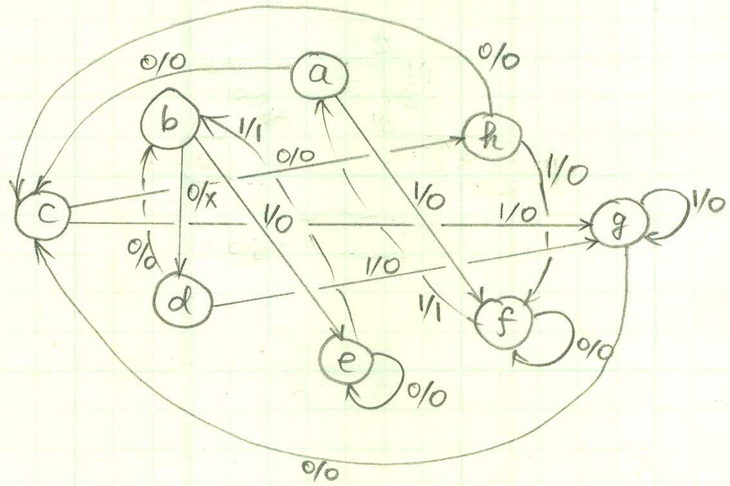
	a	b	c	d	e	f	g
b	c-d f-e						
c	~~c-h f-g~~	~~d-h e-g~~					
d	~~c-b f-g~~	~~d-b e-g~~	h-b g-g				
e	X	X	X	X			
f	X	X	X	X	e-f b-a		
g	X	X	X	X	~~e-c b-g~~	~~f-c a-g~~	
h	c-c f-f	d-c e-f	~~h-c g-f~~	~~b-c g-f~~	X	X	X

So, from the table, we have $a=b=h$, $c=d$, and $e=f$.

a. The reduced state table,

PRESENT STATE	NEXT STATE X=0	1	PRESENT OUTPUT 0	1
a	c	e	0	0
c	a	g	0	0
e	e	a	0	1
g	c	g	0	1

b. We draw a state graph for the orignal state table.



We pick the input sequence as 111, the outputs will be different if the network is initially in state "a" and "c", seperately. The output for the network initialized in state "a" is 010; for the network initialized in state "c" is 011.

16.6 ..., Do not list degenerate assignments for which two columns are identical or complements of each other, or assignments where one column is all 0's or all 1's

a. Consider a state table with three states to be realized using three J-K flip-flops. To be sure of getting the min. amout of logic, how many different state assignments must be tried? Enumerate these assignments.

THE FOLLOWING ARE ALL POSSIBLE ASSIGNMENTS WITH NO COLUMN HAVING ALL 0'S OR ALL 1'S AND NO COLUMN BEING IDENTICAL TO OTHER COLUMNS, NO COLUMN BEING COMPLEMENTED TO OTHER ONES AT ONE GROUP.

000	000	000	000	000	001	001	001	001	001	001	000	010	010
011	011	101	101	110	010	010	100	100	111	111	110	001	001
110	101	110	011	011	100	111	010	111	010	100	101	100	111

010	010	010	010	011	011	011	011	011	011	100	100
100	100	111	111	000	000	101	101	110	110	001	001
001	111	001	100	101	110	000	110	000	101	010	111

100	100	100	100	101	101	101	101	101	101	110	110
010	010	111	111	000	000	011	011	110	110	000	000
001	111	001	010	011	110	000	110	000	011	011	101

110	110	110	110	111	111	111	111	111	111
011	011	101	101	001	001	010	010	100	100
000	101	000	011	010	100	100	001	010	001

WE HAVE 48 DIFFERENT ASSIGNMENTS ABOVE. ALL OF THOSE SATISFY THE RULES.

b. For four states and three flip-flops, 29 assignments must be tried. Enumerate 10 of these, alway assigning 000 to the first state.

000	000	000	000	000	000	000	000	000	000
100	100	100	100	100	100	100	100	100	100
001	001	001	001	010	010	010	010	011	011
010	011	110	111	001	011	101	111	001	010

etc.

16.10 a. Reduce the following state table to a minimum number of states using an implication chart.

9

b. Repeat part a, using the next class method.

c. Use the guideline method to determine a suitable state assignment for the reduced table.

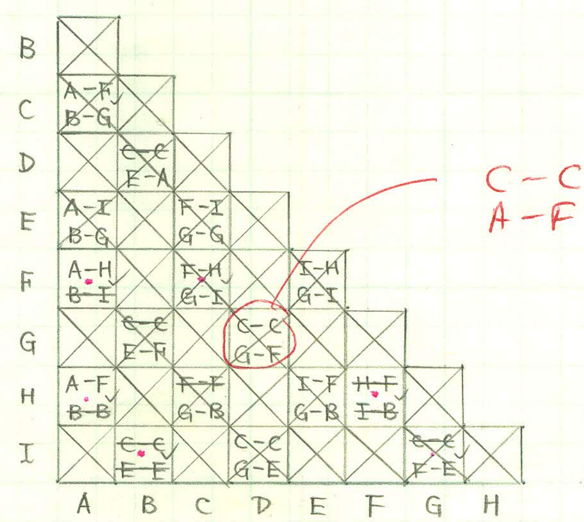
d. Realized the table using D flip-flops.

e. Realized the table using J-K flip-flops

f. Find a minimum legth input sequence which will distinguish between states B and D in the original table.

	X=0	X=1	Z
A	A	B	1
B	C	E	0
C	F	G	1
D	C	A	0
E	I	G	1
F	H	I	1
G	C	F	0
H	F	B	1
I	C	E	0

SOLUTION: (a)



∴ A = F = H   B = I   G = D

Reduced table

	X=0	X=1	Z
A	A	B	1
B	C	E	0
C	A	G	1
D	C	A	0
E	B	G	1
G	C	A	0

← G can be eliminated, although this won't change circuit complexity much, if any.

(b) WE DON'T STUDY THE NEXT CLASS METHOD.

(c) According the Guideline 1 and 2, WE have to give following group to the adjacent assignments.

Guideline 1: (A, C), (B, D, G), (C, E), (D, G)

Guideline 2: (A, B), $(C, E)_{2x}$, (A, G), $(C, A)_{3x}$, $(B, G)_{2x}$

THE ASSIGNMENT MAPS:

ST \ R	0	1
00	A^{000}	G^{100}
01	C^{001}	B^{101}
11	E^{011}	
10		D^{110}

OK

(d) & (e)

ST \ XR	00	01	11	10
00	A_A	C_G	A_G	B_A
01	A_C	C_B	E_B	G_C
10	B_E	X	X	G_E
11	X	C_D	A_D	X

R^+ (J_R, K_R)

ST \ XR	00	01	11	10
00	0	0	0	1
01	0	0	0	X
10	1	X	X	X
11	X	0	0	1

S^+

ST \ XR	00	01	11	10
00	0	0	0	0
J_S 01	0	0	1	X
K_S' 11	0	X	X	X
10	X	0	0	1

T^+ (K_T', J_T)

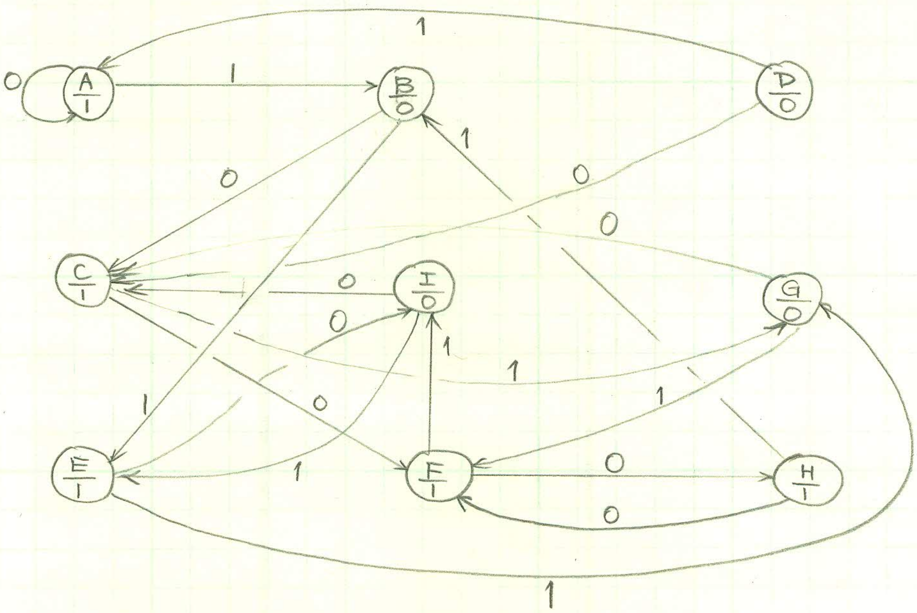
ST \ XR	00	01	11	10
00	0	1	0	1
01	0	1	1	X
11	1	X	X	X
10	X	1	0	0

(d) $D_R = R^+ = S\bar{T} + X\bar{R}$ $D_S = S^+ = XT + S\bar{R}X$ $D_T = T^+ = ST + \bar{X}R + TX + \bar{S}\bar{R}X$

(e) $J_R = X\bar{R} + S\bar{R}X$, $K_R = 1$ $J_S = \bar{S}TX$, $K_S = ST + SR$ $J_T = \bar{T}R\bar{X} + \bar{R}\bar{S}\bar{T}X$, $K_T = \bar{S}T\bar{R}$

OK

(f) WE HAVE DRAW A STATE GRAPH FOR ORIGINAL STATE TABLE,



THE MINIMUM LENGTH INPUT SEQUENCE TO DISTINGUISH B & D IS

STATE	B	E	I
INPUT	1	0	X
OUPUT	0	1	0

D	A	A
1	0	X
0	1	1

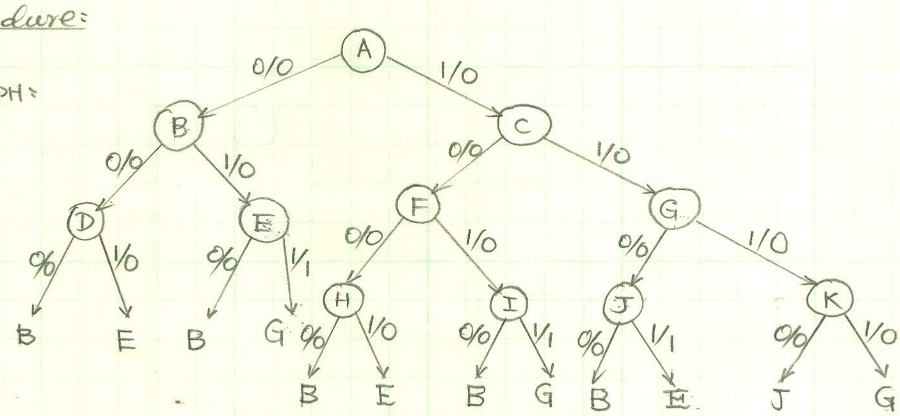
✓

17. B. Design a clocked sequential network (Fig. 17-6) which investigates an input sequence X and will produce an output of Z = 1 for any sequence ending in 1101 or 011.

10

Design Procedure:

① STATE GRAPH:



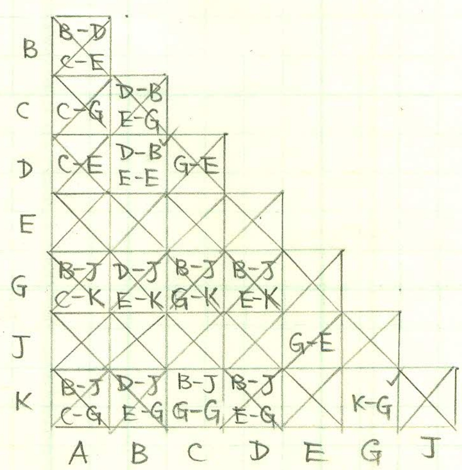
② STATE TABLE:

	X=0	X=1	X=0	1
A	B	C	0	0
B	D	E	0	0
C	~~F~~ B	G	0	0
D	B	E	0	0
E	B	G	0	1
~~F~~	~~H~~ D	~~I~~ E	0	0
G	J	K	0	0
~~H~~	B	E	0	0
~~I~~	B	G	0	1
J	B	E	0	1
K	J	G	0	0

F = B

H = D
I = E

③ USING COMPLICATION TABLE,



D = B

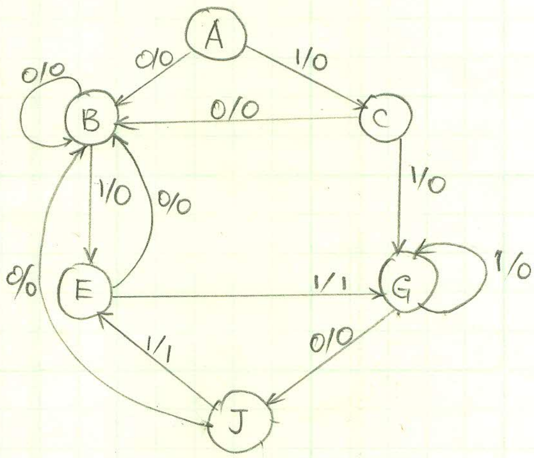
K = G

17(B) (CONT.)

④ REDUCED STATE TABLE

	$X=0$	$X=1$	0	1
A	B	C	0	0
B	B	E	0	0
C	B	G	0	0
E	B	G	0	1
G	J	G	0	0
J	B	E	0	1

⑤ REDUCED STATE GRAPH.



⑥ CHECK (i) $X=$ 0 0 1 1 0 1 1 0 1 0 1 1 0 1 0

$Z=$ 0 0 0 1 0 1 1 0 1 0 0 1 0 1 0

(ii) $X=$ 1 1 0 0 1 0 1 1 0 1 0 1 0 1 1 1 0 1 1 0 1 1 0 1

$Z=$ 0 0 0 0 0 0 0 1 0 1 0 0 0 0 1 0 0 1 1 0 1 1 0 1

(iii) $X=$ 0 0 1 1 0 0 1 1 0 1 0 1 0 1 1 0 1 0 1 0 1 1 0 1

$Z=$ 0 0 0 1 0 0 0 1 0 1 0 0 0 0 1 0 1 0 0 0 0 1 0 1

Q.E.D.

⑦ USING GUIDELINES FOR STATE ASSIGNMENT.

1. (A, B, C, E, J), (C, E, G), (B, J)

2. (B, C), $(B, E)_{2x}$, $(B, G)_{2x}$, (J, G)

3. (A, B, C, E, G, J), (A, B, C, G), (E, J)

17 B. (CONT.)

⑧ ASSIGNMENT MAPS:

bc \ a	0	1
00	A_{000}	B_{100}
01		J_{101}
11		G_{111}
10	C_{010}	E_{110}

OK

⑨ NEXT STATE MAPS:

bc \ xa	00	01	11	10
00	B_A	B_B	E_B	C_A
01		B_J	E_J	
11		J_G	G_G	
10	B_C	B_E	G_E	G_C

J_A (columns 00, 10); K_A' (columns 01, 11)

bc \ xa	00	01	11	10
00	1	1	1	0
01	X	1	1	X
11	X	1	1	X
10	1	1	1	1

a^+

J_b / K_b'

bc \ xa	00	01	11	10
00	0	0	1	1
01	X	0	1	X
11	X	0	1	X
10	0	0	1	1

b^+

J_c (rows 00, 10)

bc \ xa	00	01	11	10
00	0	0	0	0
01	X	0	0	X
11	X	1	1	X
10	0	0	1	1

c^+

$J_a = \bar{a}\bar{x} + \bar{a}b = \overline{\overline{(\bar{a}\cdot\bar{x})}\cdot\overline{(\bar{a}\cdot b)}}$

$K_a' = 1$; $K_a = 0$

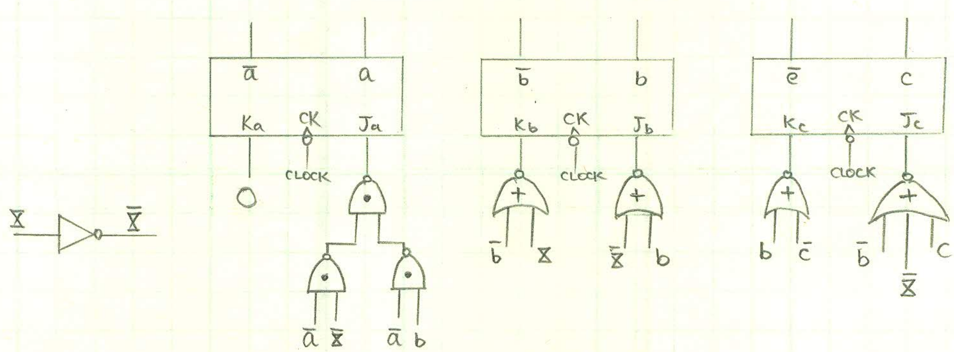
$J_b = \bar{b}x = \overline{b + \bar{x}}$

$K_b = \bar{x}b = \overline{x + \bar{b}}$

$J_c = xb\bar{c} = \overline{\bar{x} + \bar{b} + c}$

$K_b = \bar{b}c = \overline{b + \bar{c}}$

⑩ NAND NOR GATE CIRCUIT (8 GATES).



END!

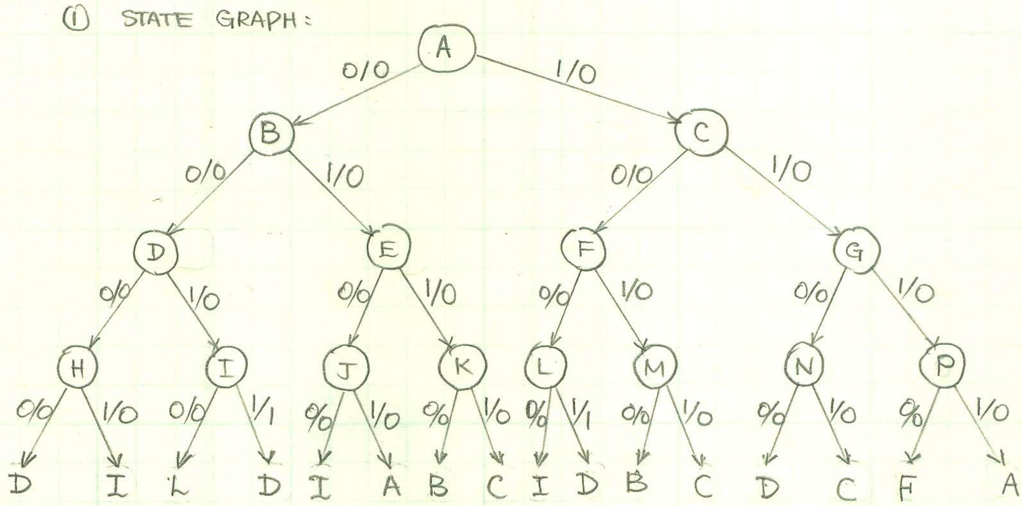
17 G. Design a clocked Mealy sequential network which investigates an input sequence X and which will produce an output of Z=1 if the total number of 1's recieived is even (consider zero 1's to be an even number of 1's) and the sequence 00 has occurred at least once.

Note: The total number of 1's received includes those received before and after 00.

Design Procedure:

* ZERO 1'S TO BE AN EVEN # OF 1'S.

① STATE GRAPH:



② STATE TABLE:

	X=0	X=1	X=0	X=1
A	B	C	0	0
B	D	E	0	0
C	F	G	0	0
D	H	I	0	0
E	J	~~K~~ A	0	0
F	L	~~M~~ A	0	0
G	N	P	0	0
H	D	I	0	0
I	L	D	0	1
J	I	A	0	0
~~K~~	~~B~~	~~C~~	~~0~~	~~0~~
L	I	D	0	1
~~M~~	~~B~~	~~C~~	~~0~~	~~0~~
N	D	C	0	0
P	F	A	0	0

A=K=M

M=K

17G. (CONT.)

③ USING COMPLICATION TABLE

	A	B	C	D	E	F	G	H	I	J	L	N
B	B-D C-E											
C	B-F C-G	D-F E-G										
D	B-H C-I	D-H E-I	F-H G-I									
E	B-J C-A	D-J E-A	F-J G-A	H-J I-A								
F	B-L C-A	D-L E-A	F-L G-A	H-L I-A	J-L A-A							
G	B-N C-P	D-N E-P	F-N G-P	H-N I-P	J-N A-P	L-N A-P						
H	B-D C-I	D-D E-I	F-D G-I	H-D I-I	J-D A-I	L-D A-I	N-D P-I					
I												
J	B-I C-A	D-I E-A	F-I G-A	H-I I-A	J-I A-A	L-I A-A	N-I P-A	D-I I-A				
L	B-I C-D	D-I E-D	F-I G-D	H-I I-D	J-I A-D	L-I A-D	N-I P-D	D-I I-D	L-I			
N	B-D C-C	D-D E-C	F-D G-C	H-D I-C	J-D A-C	L-D A-C	N-D P-C	D-D I-C		I-D A-C		
P	B-F C-A	D-F E-A	F-F G-A	H-F I-A	J-F A-A	L-F A-A	N-F P-A	D-F I-A		I-F A-A		D-F C-A

A=G

B=N

C=P=E

J=F

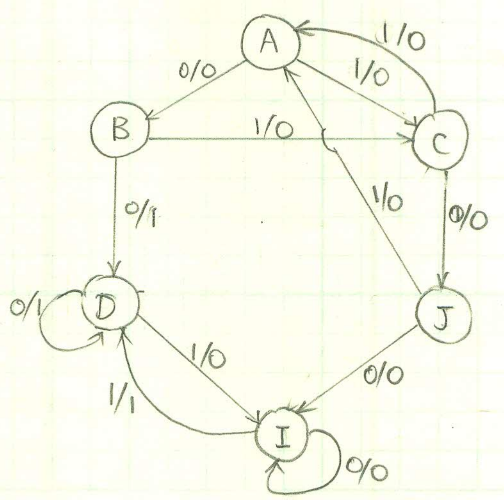
H=D

L=I

④ REDUCED STATE TABLE:

	X=0	X=1	X=0	X=1
A	B	C	0	0
B	D	C	1	0
C	J	A	0	0
D	D	I	1	0
I	I	D	0	1
J	I	A	0	0

⑤ REDUCED STATE GRAPH:



17G. (CONT.)

⑥ CHECK: (i) $X = 1\ 0\ 1\ 0\ 1\ 0\ 0\ 1\ 1\ 0\ 1$

$Z = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 1$

(ii) $X = 0\ 1\ 1\ 0\ 0\ 1\ 0\ 1\ 0\ 0$

$Z = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1\ 0\ 0$

⑦ USING GUIDELINES FOR STATE ASSIGNMENT

1. (B, D), (I, J), (A, B), (C, J)

2. (B, C), (D, C), (J, A), $(D, I)_{2x}$, (I, A)

3. (A, B, C, D, I, J), (A, B, C, D, J)

⑧ ASSIGNMENT MAPS:

bc \ a	0	1
00	A_{000}	I_{100}
01	B_{001}	D_{101}
11	C_{011}	
10	J_{010}	$_{110}$

⑨ NEXT STATE MAPS:

bc \ Xa	00	01	11	10
00	B_A	I_I	D_I	C_A
01	D_B	D_D	I_D	C_B
11	J_C	X	X	A_C
10	I_J	X	X	A_J

J_a, K_a'

bc \ Xa	00	01	11	10
00	0	1	1	1
01	1	1	1	0
11	0	x	x	0
10	1	X	X	0

J_b / K_b'

bc \ Xa	00	01	11	10
00	0	0	0	1
01	0	0	0	1
11	1	x	x	0
10	0	X	X	0

J_c

bc \ Xa	00	01	11	10
00	1	0	1	0
01	1	1	0	1
11	0	x	x	0
10	0	X	X	0

$J_a = \bar{a}\bar{b}c\bar{X} + \bar{a}b\bar{c}X + \bar{a}\bar{b}\bar{c}X$

$K_a = 0$

$J_b = \bar{a}\bar{b}X$

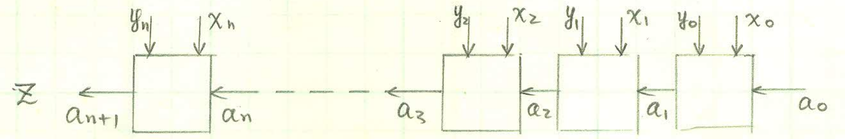
$K_b = b\bar{c} + b\bar{a}X$

$J_c = \bar{X}\bar{a}\bar{b}\bar{c} + \bar{c}aX$

$K_c = bc + c \cdot a \cdot X$

10

18.1 Two binary numbers, $X = x_n \cdots x_3 x_2 x_1 x_0$ and $Y = y_n \cdots y_3 y_2 y_1 y_0$, are to be compared by an iterative network. The comparator should compare the least significant bits first so that the intercell signals will propagate from right to left:



Only one lead should be used between each pair of cells. The output from the left end cell should be $a_{n+1} = 1$ if $X \geq Y$ and $a_{n+1} = 0$ if $X < Y$. Design a typical cell using NAND gates.

SOLUTION: FOR A TYPICAL CELL i,

a_i	x_i	y_i	a_{i+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

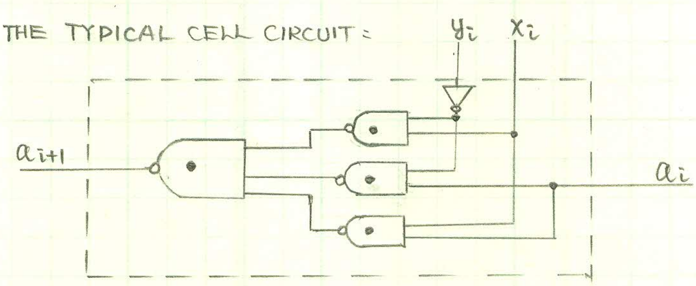
a_i \ $x_i y_i$	00	01	11	10
0	0	0	0	1
1	1	0	1	1

a_{i+1}

$$\therefore a_{i+1} = x_i \bar{y}_i + x_i a_i + \bar{y}_i a_i$$

$$= \overline{\overline{(x_i \bar{y}_i)} \cdot \overline{(x_i a_i)} \cdot \overline{(\bar{y}_i a_i)}}$$

THE TYPICAL CELL CIRCUIT:



SET: $a_0 = 1$

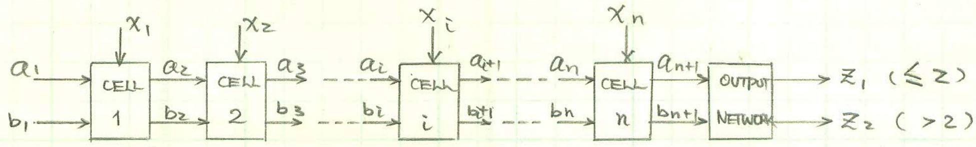
FINAL OUTPUT

$Z = a_{n+1}$

18.3 An iterative network has a form similar to Fig. 18-4. The output Z is to be 1 iff the total number of x-inputs which are 1 is an odd number greater than 2.

Derive the equations and a NAND-gate network for a typical cell and the output network. Specify a_1 and b_1 and simplify the first cell.

SOLUTION:



WE DEFINE S_0 REPRESENTS TOTAL # OF 1's = 0 ($a_i b_i = 00$)

S_1 REPRESENTS TOTAL # OF 1's = 1 ($a_i b_i = 01$)

S_2 REPRESENTS TOTAL # OF 1's = 2 OR >2 & even ($a_i b_i = 10$)

S_3 REPRESENTS TOTAL # OF 1's > 2 & ODD ($a_i b_i = 11$)

STATE TABLE FOR CELL i

S_i	S_{i+1}: $x_i = 0$	1	Z
S_0	S_0	S_1	0
S_1	S_1	S_2	0
S_2	S_2	S_3	0
S_3	S_3	S_2	1

TRANSITION TABLE FOR CELL i

$a_i b_i$	$a_{i+1} b_{i+1}$: $x_i = 0$	1	Z
0 0	0 0	0 1	0
0 1	0 1	1 0	0
1 0	1 0	1 1	0
1 1	1 1	1 0	1

x_i \ $a_i b_i$	00	01	11	10
0	0	0	1	1
1	0	1	1	1

a_{i+1}

x_i \ $a_i b_i$	00	01	11	10
0	0	1	1	0
1	1	0	0	1

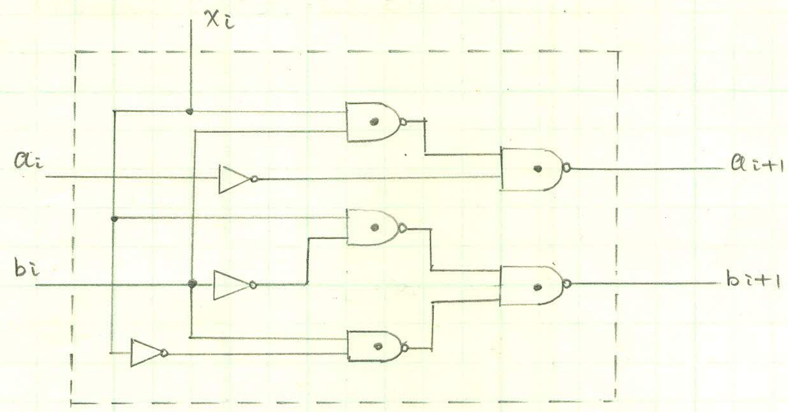
b_{i+1}

$$a_{i+1} = a_i + b_i x_i$$

$$= \overline{\overline{a_i} \cdot \overline{(b_i x_i)}}$$

$$b_{i+1} = b_i \overline{x_i} + \overline{b_i} x_i$$

18-3 (CONT.) TYPICAL CELL CIRCUIT:

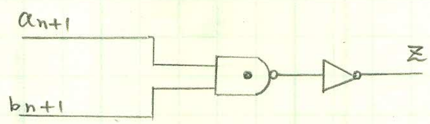


THE OUTPUT NETWORK:

$b_{n+1} \backslash a_{n+1}$	0	1
0	0	0
1	0	1

Z

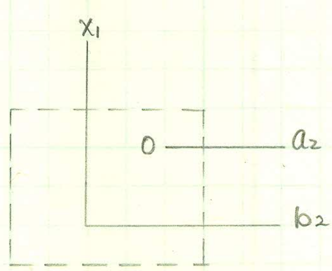
$$Z = a_{n+1} \cdot b_{n+1} = \overline{\overline{a_{n+1} b_{n+1}}}$$



FOR CELL 1: $a_1 = 0$ $b_1 = 0$

$\therefore$ $a_2 = 0$ $b_2 = x_i$

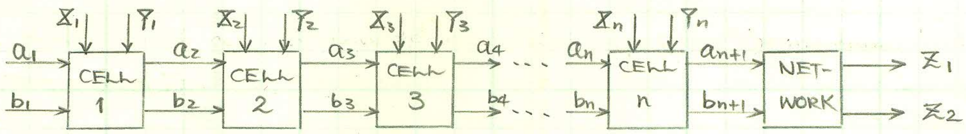
THE SIMPLIFIED CIRCUIT FOR THE FIRST CELL



18.7. EACH CELL HAS INPUTS X_i & Y_i, NETWORK HAS TWO outputs Z_1 & Z_2.

$Z_1 = 1$ IF $X_i = Y_i$ IN EVERY CELL. $Z_2 = 1$ IF X_i AND Y_i are complements in every cell.

SOLUTION: a. Specify the form of the network.



b)

a_ib_i	S_i	S_{i+1}: $X_iY_i=00$	01	10	11	Z_1	Z_2
(00)	S_0	S_0	S_2	S_2	S_0	1	0
(01)	S_1	S_2	S_1	S_1	S_2	0	1
(11)	S_2	S_2	S_2	S_2	S_2	0	0

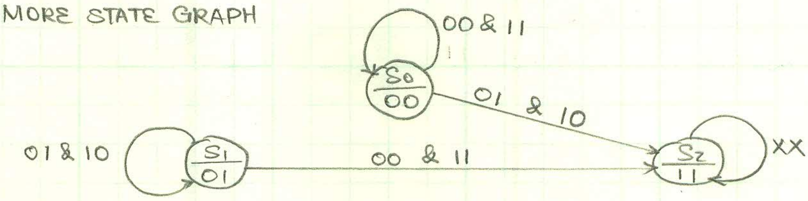
* S_0 REPRESENTS ALL X_i & Y_i ON LEFT OF CELL i ARE EQUAL

S_1 REPRESENTS ALL X_i & Y_i ON LEFT OF CELL i ARE COMPLEMENTS IN EVERY CELL.

S_1 IS BOTH UNEQUAL AND IMCOMPLEMENTAL.

(THIS IS NOT GOOD FOR CELL 1, HOWEVER, WE CAN SIMPLIFY PART e)

MORE STATE GRAPH



C) DESIGN A TYPICAL CELL USING ONLY NAND GATES. ASSIGN 00 TO INITIAL STATE.

a_ib_i	$a_{i+1}b_{i+1}$: $X_iY_i=00$	01	10	11	Z_1	Z_2
0 0	00	11	11	00	1	0
0 1	11	01	01	11	0	1
1 1	11	11	11	11	0	0
1 0	XX	XX	XX	XX	X	X

a_ib_i \ X_iY_i	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	1	1	1	1
10	X	X	X	X

a_{i+1}

a_ib_i \ X_iY_i	00	01	11	10
00	0	1	0	1
01	1	1	1	1
11	1	1	1	1
10	X	X	X	X

b_{i+1}

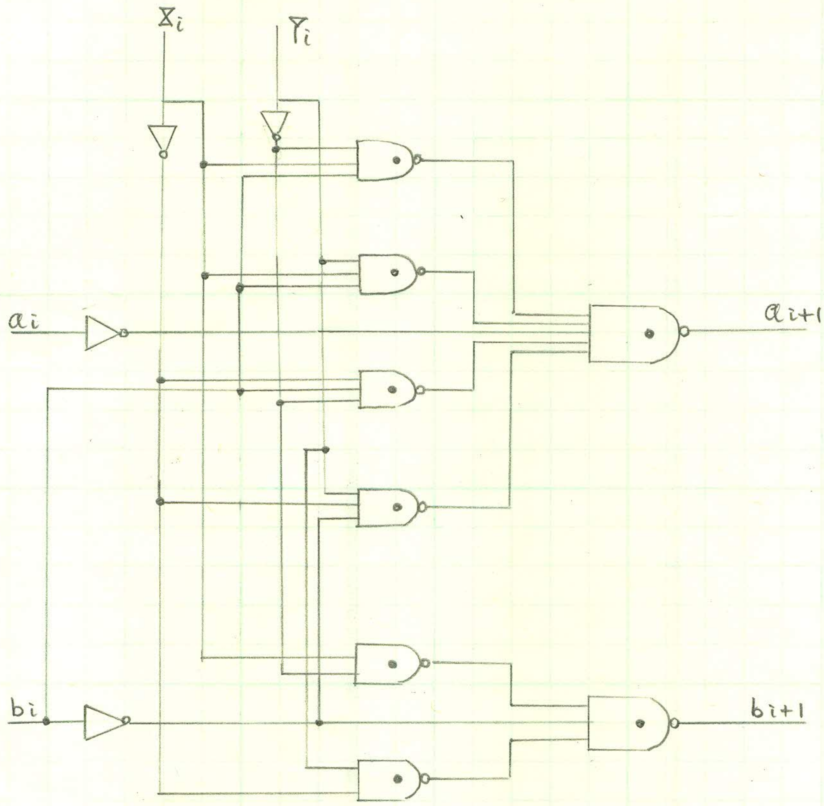
$$a_{i+1} = a_i + b_i\bar{X}_i\bar{Y}_i + \bar{b}_i\bar{X}_iY_i + b_iX_iY_i + \bar{b}_iX_i\bar{Y}_i$$

$$= \overline{\bar{a}_i \cdot (\overline{b_i\bar{X}_i\bar{Y}_i})(\overline{\bar{b}_i\bar{X}_iY_i}) \cdot (\overline{b_iX_iY_i})(\overline{\bar{b}_iX_i\bar{Y}_i})}$$

$$b_{i+1} = b_i + \bar{X}_iY_i + X_i\bar{Y}_i$$

$$= \overline{\bar{b}_i \cdot (\overline{\bar{X}_iY_i})(\overline{X_i\bar{Y}_i})}$$

THE CELL



d) THE OUTPUT NETWORK :

a_{n+1}	b_{n+1}	Z_1	Z_2
0	0	1	0
0	1	0	1
1	1	0	0
1	0	X	X

b_{n+1} \ a_{n+1}	0	1
0	1	X
1	0	0

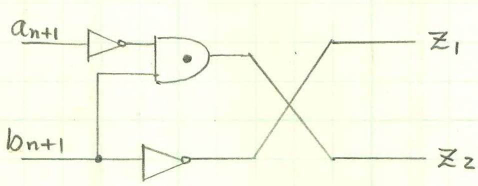
Z_1

b_{n+1} \ a_{n+1}	0	1
0	0	X
1	1	0

Z_2

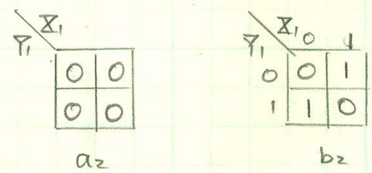
$Z_1 = \bar{b}_{n+1}$

$Z_2 = \bar{a}_{n+1} b_{n+1}$



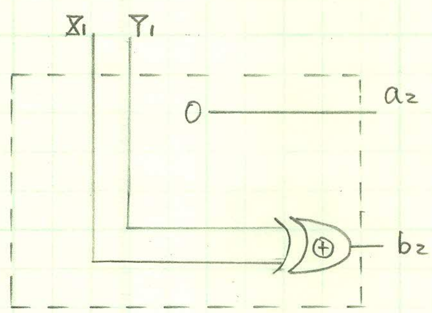
e) SIMPLIFY THE FIRST CELL IF POSSIBLE (SURE, I HAVE TO REDESIGN FIRST CELL)

X_1	Y_1	a_2	b_2
0	0	0	0
0	1	0	1
1	0	0	1
1	1	0	0

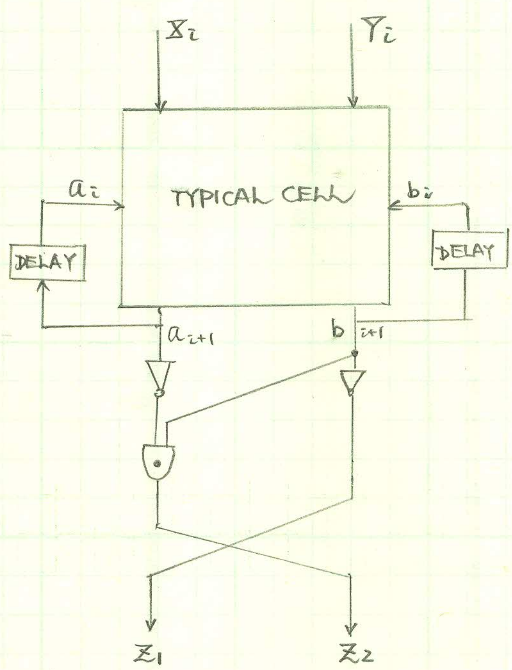


$a_2 = 0$ $\qquad$ $b_2 = \bar{X}_1 Y_1 + \bar{Y}_1 X_1 = X_1 \oplus Y_1$

THE FIRST CELL (a_1, b_1 ARE NOT NEEDED)



f).



(i > 1)

SET $a_1 = 0$

$b_1 = X_1 \oplus Y_1$

17.D DESIGN a sequential network (Fig. 17-6) which adds six ··· (PAGE 392)

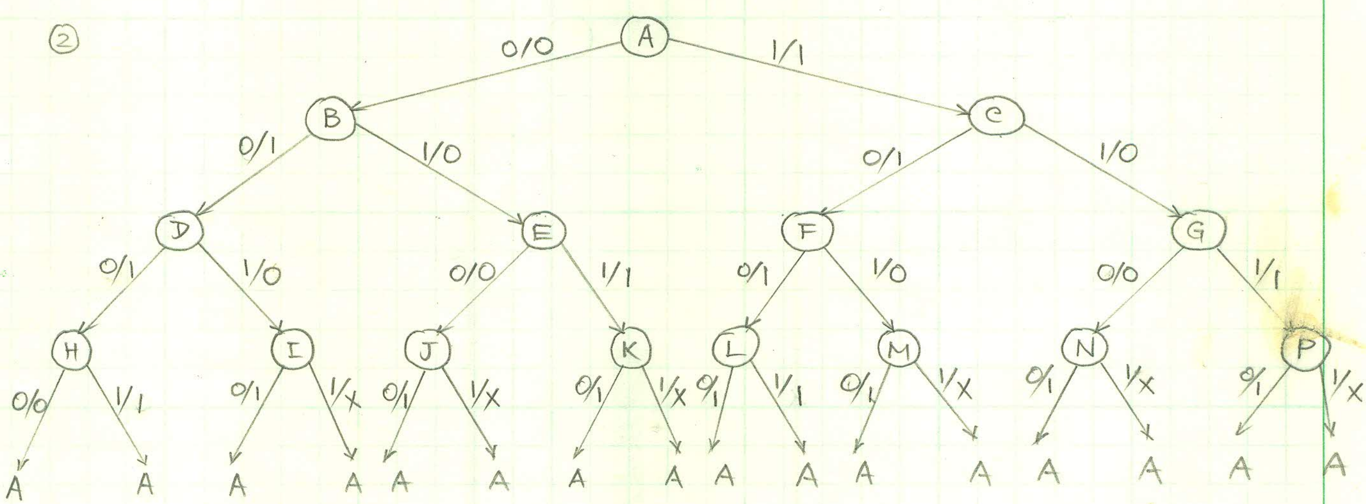
10

ADDS SIX TO A BINARY NUMBER IN THE RANGE 0000 THROUGH 1001.

①

INPUT	SIX	OUTPUT
0 0 0 0	0 1 1 0	0 1 1 0
0 0 0 1		0 1 1 1
0 0 1 0		1 0 0 0
0 0 1 1		1 0 0 1
0 1 0 0		1 0 1 0
0 1 0 1		1 0 1 1
0 1 1 0		1 1 0 0
0 1 1 1		1 1 0 1
1 0 0 0		1 1 1 0
1 0 0 1		1 1 1 1
1 0 1 0		X X X X
1 0 1 1		X X X X
1 1 0 0		X X X X
1 1 0 1		X X X X
1 1 1 0		X X X X
1 1 1 1		X X X X

②



③ REDUED BY USING ROW MATCHING METHOD.

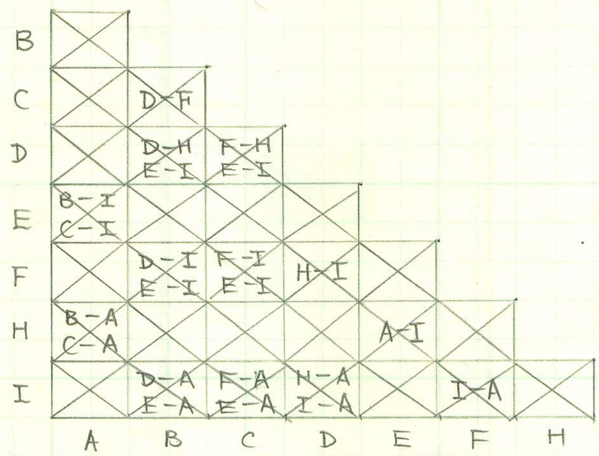
17.D (CONT.)

STATE	NEXT STATE x=0	NEXT STATE x=1	OUTPUT x=0	OUTPUT x=1
A	B	C	0	1
B	D	E	1	0
C	F	~~G~~ E	1	0
D	H	I	1	0
E	~~J~~ I	~~K~~ I	0	1
F	~~L~~ I	~~M~~ I	1	0
~~G~~	~~N~~ I	~~P~~ I	0	1
H	A	A	0	1
I	A	A	1	X
~~J~~	A	A	1	X
~~K~~	A	A	1	X
~~L~~	A	A	1	1
~~M~~	A	A	1	X
~~N~~	A	A	1	X
~~P~~	A	A	1	X

E=G

I=J=K=L=M=N=P

④

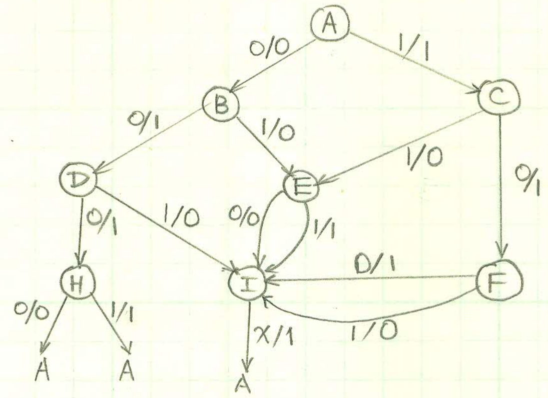


⑤ REDUCED STATE TABLE

	x=0	x=1	x=0	x=1
A	B	C	0	1
B	D	E	1	0
C	F	E	1	0
D	H	I	1	0
E	I	I	0	1
F	I	I	1	0
H	A	A	0	1
I	A	A	1	x

Reduce further?

⑥ STATE GRAPH



⑦ STATE ASSIGNMENT

(i) (E, F), $(H, I)_{2X}$, (B, C), (D, E, F)

(ii) (B, C), (D, E), (F, E), (H, I)

(iii) (B, C, D, F, I), (A, E, H), (A, E, H), (B, C, D, F)

c \ ab	00	01	11	10
0	A_{000}	H_{010}	B_{110}	I_{100}
1	E_{001}	F_{011}	C_{110}	D_{101}

ab \ Xc	00	01	11	10
00	B_A	I_E	I_E	C_A
01	A_H	I_F	I_F	A_H
11	D_B	F_C	E_C	E_B
10	A_I	H_D	I_D	A_I

ab \ Xc	00	01	11	10
00	1	1	1	1
01	0	1	1	0
11	1	0	0	0
10	0	0	1	0

a^+

$J_a = \bar{a}\bar{b}\bar{c} + ab\bar{c}\bar{x}$

$K_a = abc + bc\bar{x}$

ab \ Xc	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	1	0	0
10	0	1	0	0

b^+

$J_b = \bar{a}\bar{b}\bar{c}$

$K_b = ax + a\bar{c}$

ab \ Xc	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

c^+

$J_c = 0$

$K_c = \bar{b}$

ab \ Xc	00	01	11	10
00	0 A	0 E	1 E	1 A
01	0 H	1 E	0 E	1 H
11	1 B	1 C	0 C	0 B
10	1 I	1 D	0 D	X I

Z

$$Z = a\bar{x} + bc\bar{x} + \bar{a}\bar{c}x + \bar{a}\bar{b}x$$

(8) CIRCUIT

$$J_a = \overline{\bar{a}\bar{b}\bar{c} + abc\bar{x}} = \overline{\overline{(\bar{a}\bar{b}\bar{c})} \cdot \overline{(abc\bar{x})}} = \overline{\overline{J_b}\;\overline{(abc\bar{x})}}$$

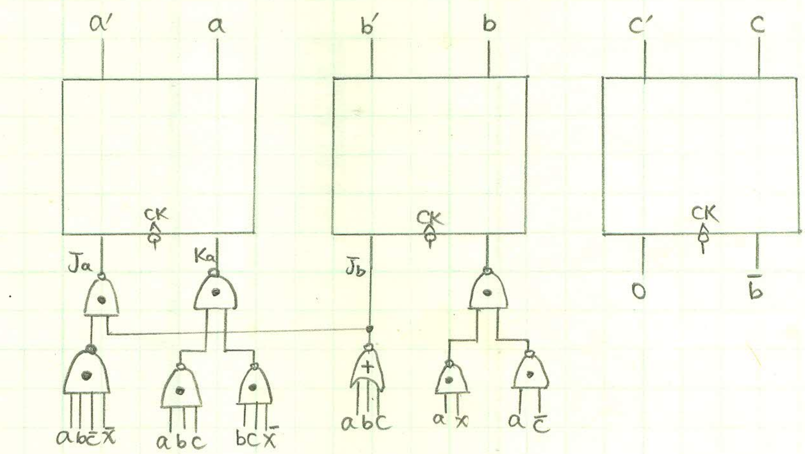
$$K_a = \overline{\overline{(abc)} \cdot \overline{(bc\bar{x})}}$$

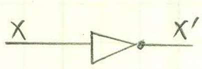
$$J_b = \overline{a + b + c}$$

$$K_b = \overline{\overline{(ax)}\;\overline{(a\bar{c})}}$$

$$J_c = 0$$

$$K_c = \bar{b}$$





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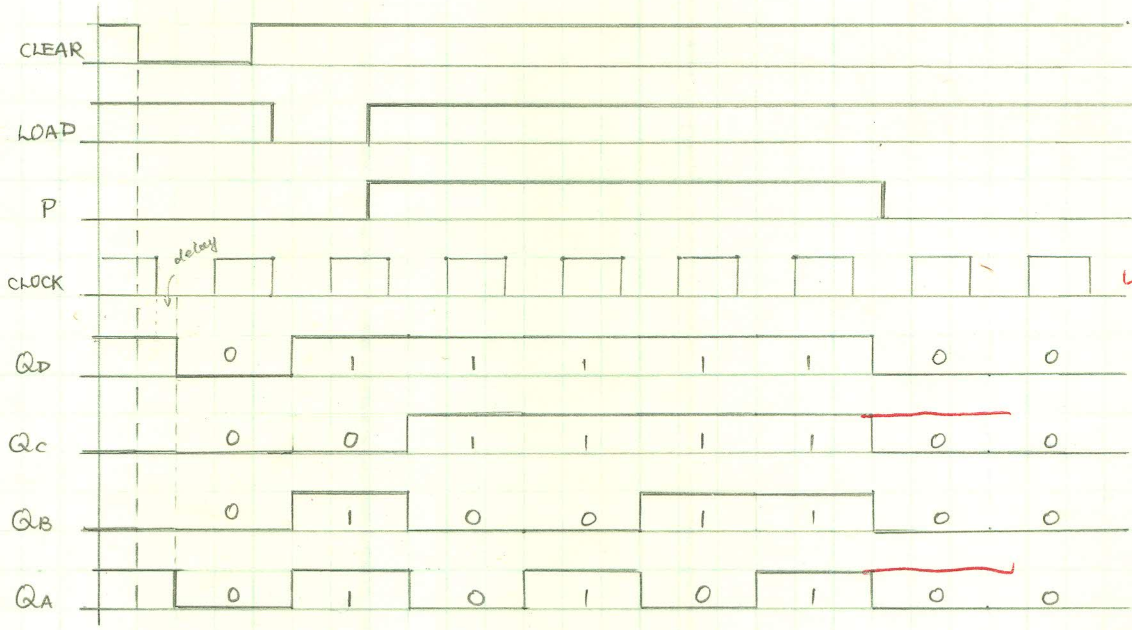
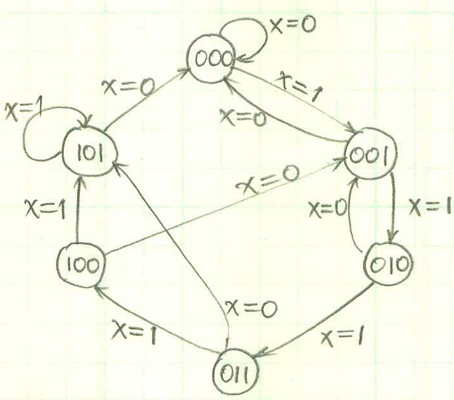
19.3 Complete the following timing diagram for a 74S163 counter. Assume that

$D_D = D_B = D_A = 1$, $D_C = 0$, $T = 1$



Use rising clock edges

19.6 Realize the given state graph using a 74S163 counter with added gates.



CLEAR

BA \ XC	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	1	X	1	X
10	1	X	1	X

LOAD

BA \ XC	00	01	11	10
00	X	0	1	1
01	X	X	1	1
11	0	X	1	X
10	0	X	1	X

D_C

BA \ XC	00	01	11	10
00	X	0	X	X
01	X	X	X	X
11	1	X	X	X
10	0	X	X	X

D_B

BA \ XC	00	01	11	10
00	X	0	X	X
01	X	X	X	X
11	0	X	X	X
10	0	X	X	X

D_A

BA \ XC	00	01	11	10
00	X	1	X	X
01	X	X	X	X
11	1	X	X	X
10	1	X	X	X

PT

BA \ XC	00	01	11	10
00	X	X	1	1
01	X	X	1	0
11	X	X	1	X
10	X	X	1	X

X C B A	$C^+ B^+ A^+$	CLEAR	LOAD	$D_C D_B D_A$	PT
0 0 0 0	0 0 0	0	X	X X X	X
0 0 0 1	0 0 0	0	X	X X X	X
0 0 1 0	0 0 1	1	0	0 0 1	X
0 0 1 1	1 0 1	1	0	1 0 1	X
0 1 0 0	0 0 1	1	0	0 0 1	X
0 1 0 1	0 0 0	0	X	X X X	X
0 1 1 0	X X X	X	X	X X X	X
0 1 1 1	X X X	X	X	X X X	X
1 0 0 0	0 0 1	1	1	X X X	1
1 0 0 1	0 1 0	1	1	X X X	1
1 0 1 0	0 1 1	1	1	X X X	1
1 0 1 1	1 0 0	1	1	X X X	1
1 1 0 0	1 0 1	1	1	X X X	1
1 1 0 1	1 0 1	1	1	X X X	0
1 1 1 0	X X X	X	X	X X X	X
1 1 1 1	X X X	X	X	X X X	X

$CLEAR = B + \bar{X} + C\bar{B}\bar{A}$

$LOAD = X$

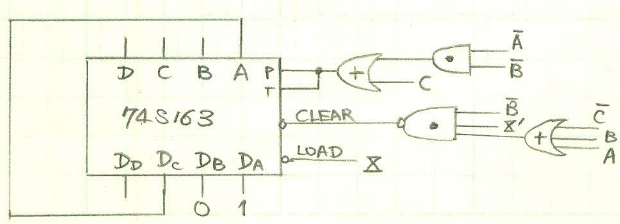
$D_C = A$

$D_B = 0$

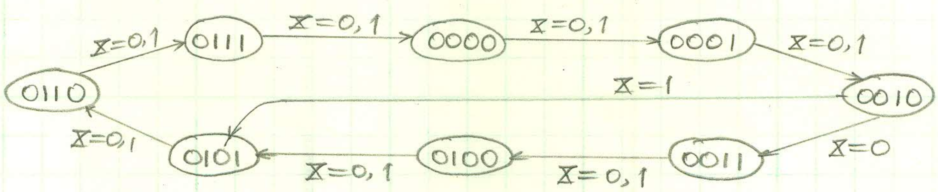
$D_A = 1$

$PT = C + \bar{B}\bar{A}$

REALIZED CIRCUIT:



19.5 Realize the given state graph using a 74S163 counter with added gates. Note that in state 0010, if X=1, the counter must be loaded with 0101. Take advantage of the fact that the LOAD signal overrides the count.



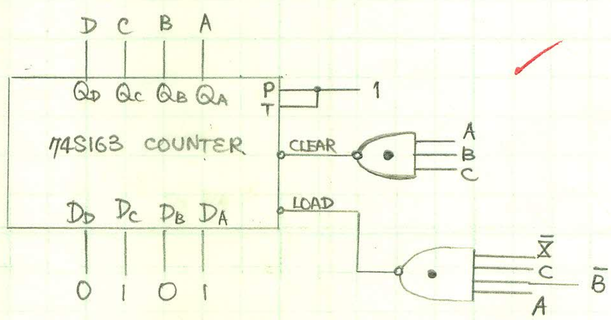
X	C	B	A	C^+	B^+	A^+	CLEAR	LOAD	D_C	D_B	D_A	PT
0	0	0	0	0	0	1	1	1	X	X	X	1
0	0	0	1	0	1	0	1	1	X	X	X	1
0	0	1	0	0	1	1	1	1	X	X	X	1
0	0	1	1	1	0	0	1	1	X	X	X	1
0	1	0	0	1	0	1	1	1	X	X	X	1
0	1	0	1	1	1	0	1	1	X	X	X	1
0	1	1	0	1	1	1	1	1	X	X	X	1
0	1	1	1	0	0	0	0	X	X	X	X	X
1	0	0	0	0	0	1	1	1	X	X	X	1
1	0	0	1	0	1	0	1	1	X	X	X	1
1	0	1	0	1	0	1	1	0	1	0	1	X
1	0	1	1	1	0	0	1	1	X	X	X	1
1	1	0	0	1	0	1	1	1	X	X	X	1
1	1	0	1	1	1	0	1	1	X	X	X	1
1	1	1	0	1	1	1	1	1	X	X	X	1
1	1	1	1	0	0	0	0	X	X	X	X	X

✓

$PT = 1$, $D_C = 1$, $D_B = 0$, $D_A = 1$, $D_D = 0$

$CLEAR = \bar{C} + \bar{B} + \bar{A}$, $LOAD = \bar{X} + \bar{C} + B + \bar{A}$

THE REALIZED CIRCUIT:



✓

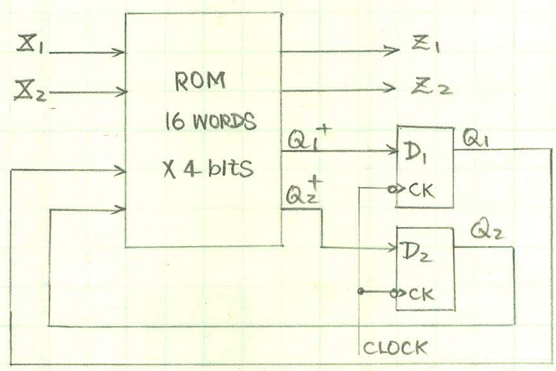
19.7 Draw a block diagram with shows how a ROM and D flip-flops could be connected to realize Table 14-4 (P. 307). Specify the truth table for the ROM using a straight binary state assignment.

10

Table 14-4:

PRE. STATE		NEXT STATE X_1X_2=00	01	10	11	PRESENT OUTPUT (Z_1Z_2) 00	01	10	11
00	S_0	S_3(11)	S_2(10)	S_1(01)	S_0(00)	00	10	11	01
01	S_1	S_0(00)	S_1(01)	S_2(10)	S_3(11)	10	10	11	11
10	S_2	S_3(11)	S_0(00)	S_1(01)	S_1(01)	00	10	11	01
11	S_3	S_2(10)	S_2(10)	S_1(01)	S_0(00)	00	00	01	01

BLOCK DIAGRAM:



TRUTH TABLE:

X_1	X_2	Q_1	Q_2	Z_1	Z_2	D_1	D_2
0	0	0	0	0	0	1	1
0	0	0	1	1	0	0	0
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	1	0	1	0
0	1	0	1	1	0	0	1
0	1	1	0	1	0	0	0
0	1	1	1	0	0	1	0
1	0	0	0	1	1	0	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	1	1	1	1
1	1	1	0	0	1	0	1
1	1	1	1	0	1	0	0

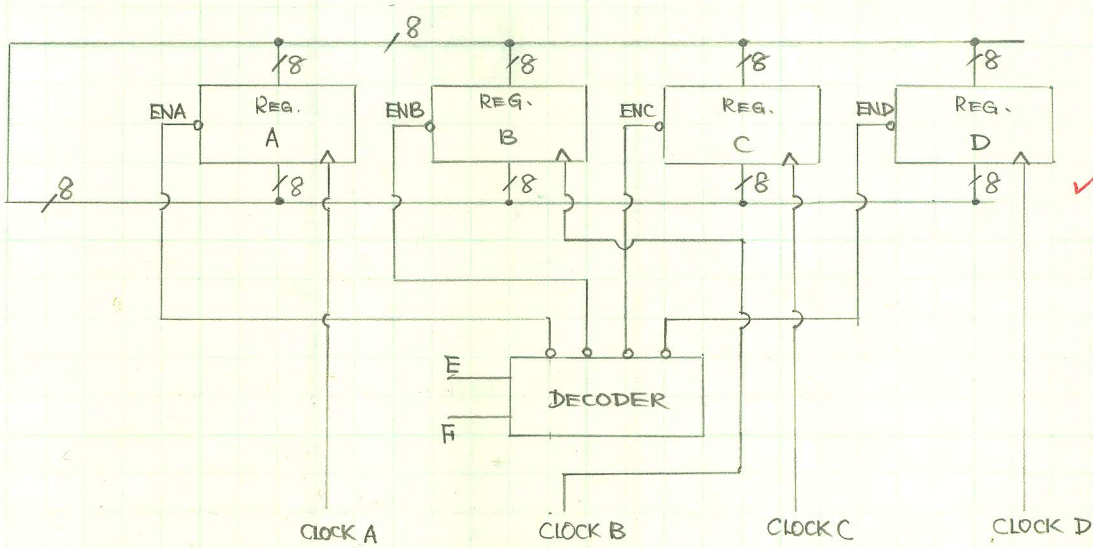
19.9 A digital system contains four 74LS374 octal D flip-flop registers. The inputs and outputs of all four registers are connected to a common bus so that the contents of any register can be loaded into any other register. A decoder is used to selectively enable the register outputs, and each register can be clocked separately.

a. Draw a block diagram of the system.

b. What should be the decoder inputs and which register(s) should be clocked in order to load the contents of register B into register A? In order to load the contents of register A into both registers C and D?

---

a. THE BLOCK DIAGRAM OF THE SYSTEM:



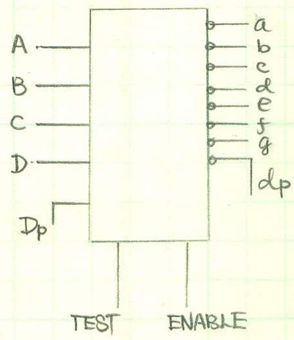
b. FOR LOADING B INTO A, DECODER INPUTS EF = 01 & REGISTER A MUST BE CLOCKED.

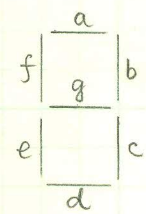
FOR LOADING A INTO BOTH C & D, DECODER INPUTS EF = 00, AND REGISTERS C & D MUST BE CLOCKED.

10

PROBLEM 19.7 (DONE IN H.W. 15)

PROBLEM 2 : Use a PAL16L8 to make a BCD-7-SEG decoder with "0" turning on LED segments.





A	B	C	D	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	×	×	×	×	×	×	×
1	0	1	1	×	×	×	×	×	×	×
1	1	0	0	×	×	×	×	×	×	×
1	1	0	1	×	×	×	×	×	×	×
1	1	1	0	×	×	×	×	×	×	×
1	1	1	1	×	×	×	×	×	×	×

THE CIRCUIT REALIZATION IS GIVEN ON NEXT PAGE.

Homework No: 16 EE410 Fundamentals of Systems Ben Chen 2.

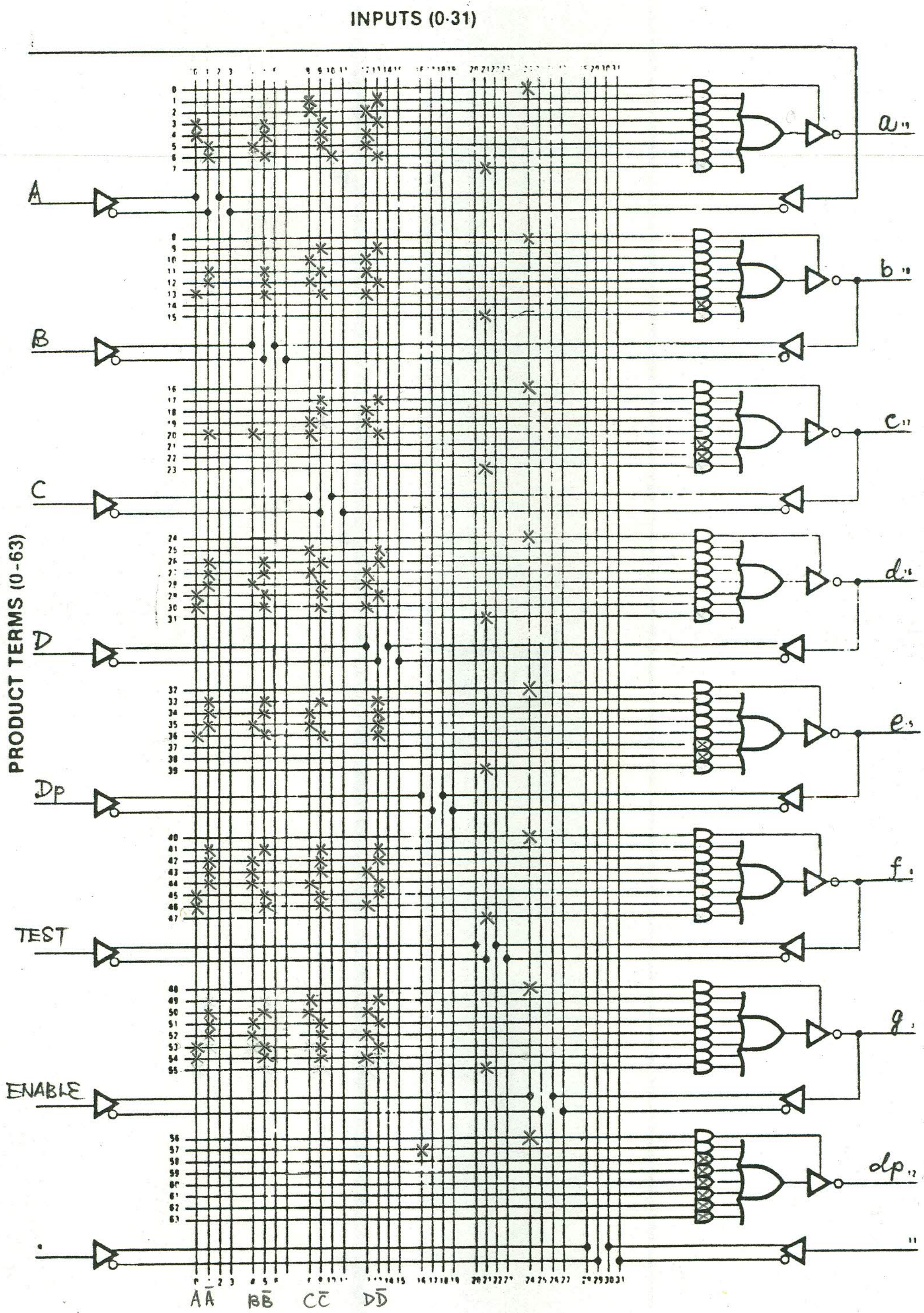


FIGURE 3-50. Logic Diagram, PAL16L8.

19-10 a. Realize the state table of Fig. 16-13 using a 16R4 PAL. (See Fig. 16-14(b) for next state equations.) Mark X's on a copy of the 16R4 diagram to indicate the fuse pattern.

b. Realize the state table of 15-5 using a 16R4 PAL. Use a straight binary state assignment ($S_0 = 000$, $S_1 = 001$ etc.)

SOLUTION: a. From Fig. 16-14 (b), we have the next state equations:

$$A^+ = D_A = \bar{X}, \quad B^+ = D_B = \bar{X}\bar{C} + \bar{A}C + \bar{A}B, \quad C^+ = D_C = A + X\bar{B}$$

However, the outputs of D Flip-Flops in PAL 16R4 are inverted. So, we have the inputs of the flip-flops,

$$D_A = X, \quad D_B = \overline{\bar{X}\bar{C} + \bar{A}C + \bar{A}B} = (X + C)\cdot(A + \bar{C})\cdot(A + \bar{B})$$

$$= (XA + X\bar{C} + CA)(A + \bar{B})$$

$$= XA + XA\bar{C} + CA + XA\bar{B} + X\bar{B}\bar{C} + CA\bar{B}$$

$$D_C = \overline{A + X\bar{B}}$$

$$= \bar{A}\cdot(\bar{X} + B) = \bar{A}\bar{X} + \bar{A}B.$$

THE CIRCUIT REALIZATION IS ON PAGE THREE.

b. Assign $S_0 = 000$, $S_1 = 001$, $S_2 = 010$, $S_3 = 011$, $S_4 = 100$, $S_5 = 101$

Redraw Table 15-5 with D-Flip-flops:

TO BE CONTINUED ON NEXT PAGE!

X_1	X_2	A	B	C	A^+	B^+	C^+	D_A	D_B	D_C		Z
0	0	0	0	0	0	0	0	1	1	1	✓	0
0	0	0	0	1	0	0	1	1	1	0		1
0	0	0	1	0	0	0	0	1	1	1	✓	0
0	0	0	1	1	0	0	1	1	1	0		1
0	0	1	0	0	0	0	0	1	1	1		0
0	0	1	0	1	0	0	1	1	1	0		1
0	0	1	1	0	x	x	x	x	x	x		x
0	0	1	1	1	x	x	x	x	x	x		x
0	1	0	0	0	0	1	0	1	0	1	✓	0
0	1	0	0	1	0	1	1	1	0	0		1
0	1	0	1	0	0	1	0	1	0	1	✓	0
0	1	0	1	1	0	1	1	1	0	0		1
0	1	1	0	0	0	1	1	1	0	0		0
0	1	1	0	1	0	1	0	1	0	1		1
0	1	1	1	0	x	x	x	x	x	x		x
0	1	1	1	1	x	x	x	x	x	x		x
1	0	0	0	0	1	0	0	0	1	1	✓	0
1	0	0	0	1	1	0	1	0	1	0		1
1	0	0	1	0	1	0	0	0	1	1	✓	0
1	0	0	1	1	1	0	1	0	1	0		1
1	0	1	0	0	1	0	0	0	1	1		0
1	0	1	0	1	1	0	1	0	1	0		1
1	0	1	1	0	x	x	x	x	x	x		x
1	0	1	1	1	x	x	x	x	x	x		x
1	1	0	0	0	0	0	0	1	1	1	✓	0
1	1	0	0	1	0	0	1	1	1	0		1
1	1	0	1	0	0	0	0	1	1	1	✓	0
1	1	0	1	1	0	0	0	1	1	1		1
1	1	1	0	0	0	0	1	1	1	0		0
1	1	1	0	1	0	0	1	1	1	0		1
1	1	1	1	0	x	x	x	x	x	x		x
1	1	1	1	1	x	x	x	x	x	x		x

$$D_A = \bar{X}_1 + X_2$$

$$D_B = X_1 + \bar{X}_2$$

$$D_C = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{X}_1\bar{X}_2A\bar{B}\bar{C} + \bar{X}_1X_2A\bar{B}C + X_1\bar{X}_2A\bar{B}\bar{C} + X_1X_2\bar{A}BC$$

$$Z = C$$

THE CIRCUIT REALIZATION IS ON PAGE 4.

Homework N: 17 Ben Page 3

The circuit realization for 19-10. a.

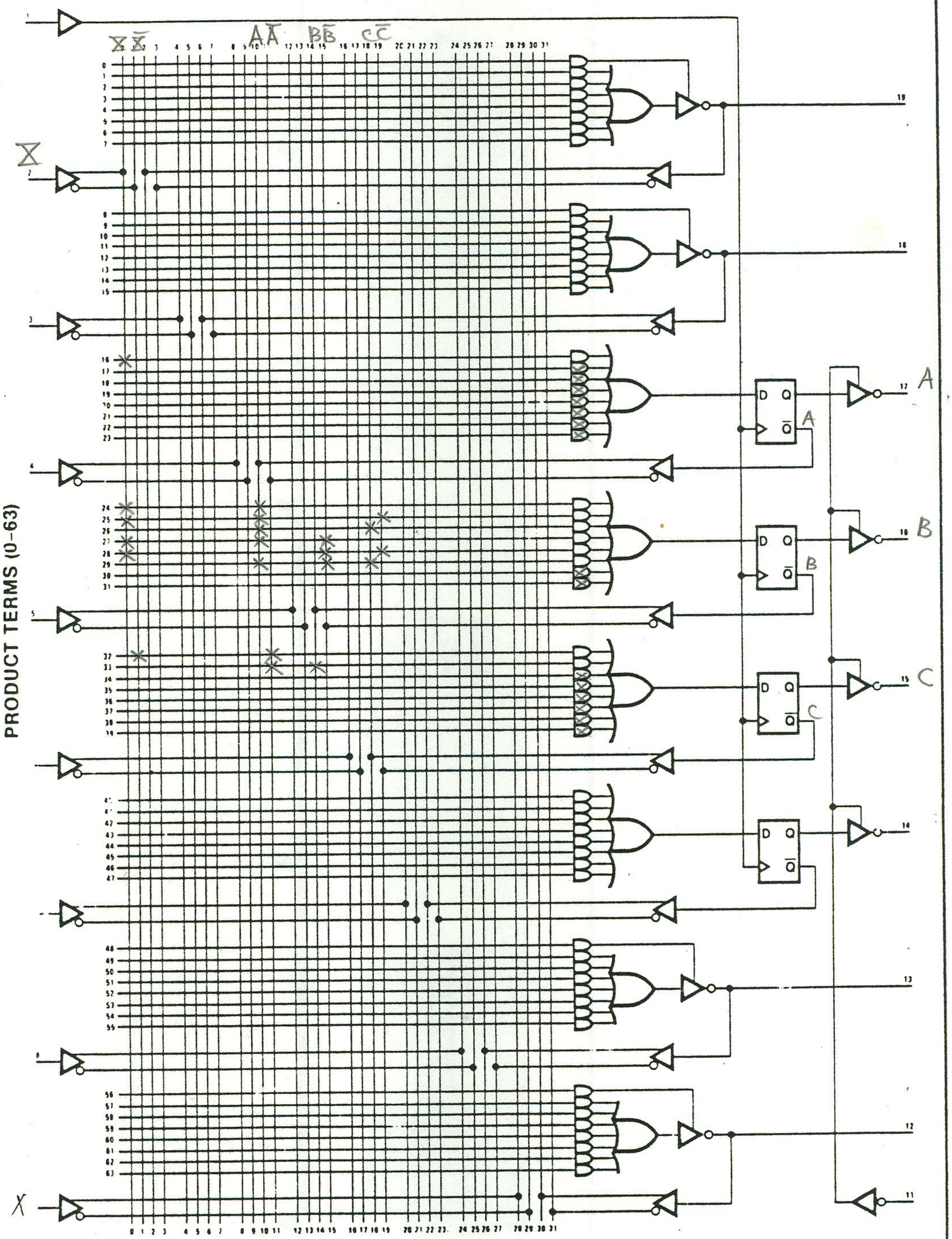


FIGURE 3-56. Logic Diagram, PAL16R4.

Homework NO: 17 . Ben

The circuit realization for 19-10.b

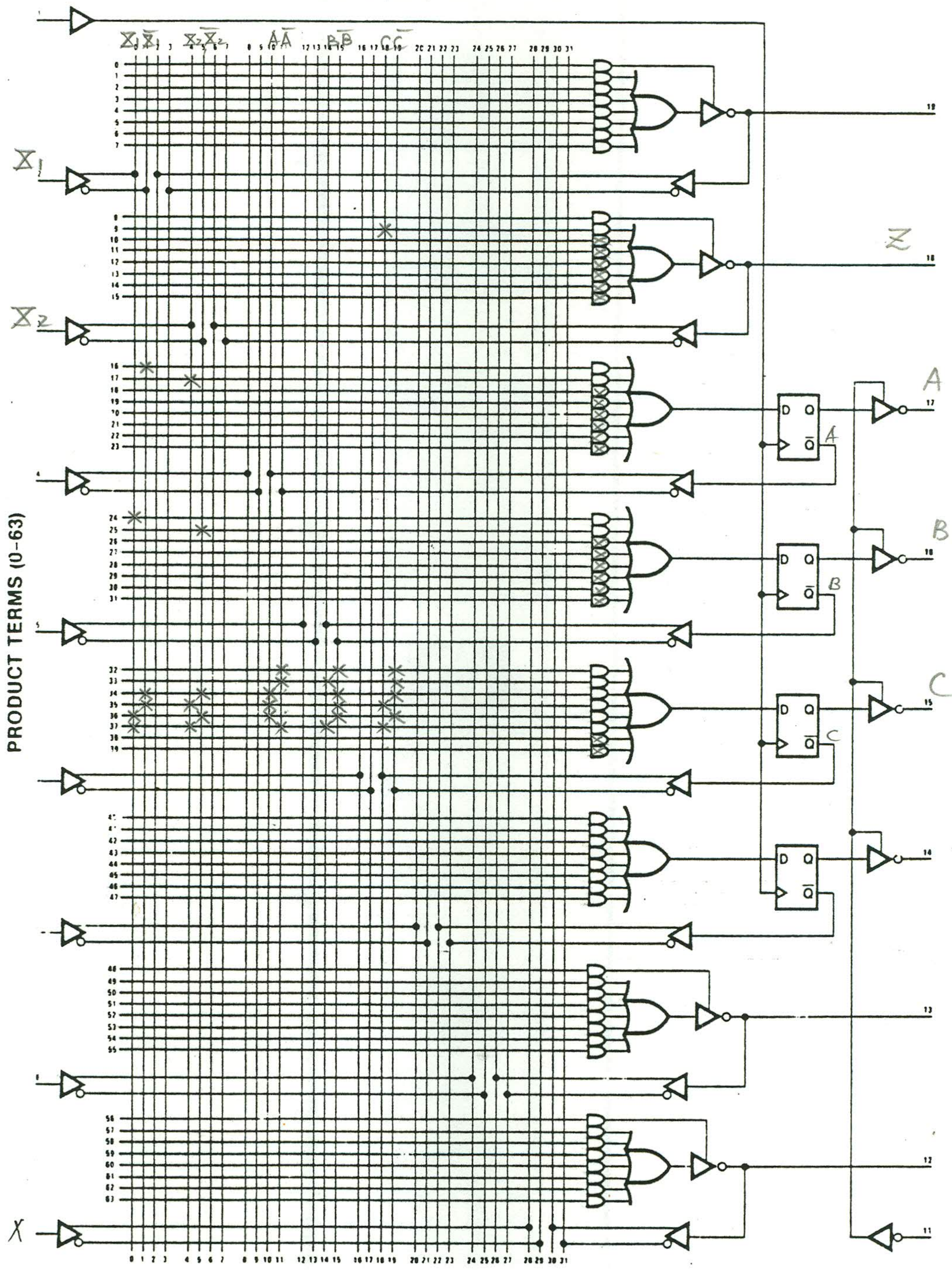
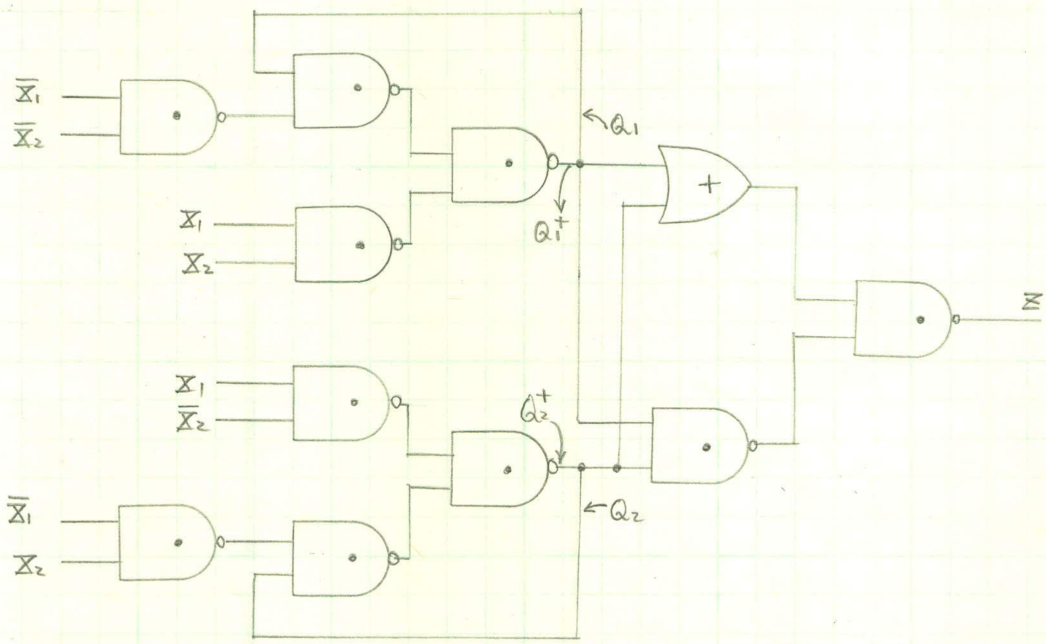


FIGURE 3-56. Logic Diagram, PAL16R4.

23.3 Analyze the following network using a flow table. What is the output sequence for the following input sequence: $X_1X_2 = 00, 10, 11, 01, 11, 10, 00, 01, 00$?



SOLUTION: FROM THE NETWORK ABOVE, WE HAVE

$$Q_1^+ = \overline{\overline{\overline{X}_1\cdot\overline{X}_2\cdot Q_1}\cdot\overline{X_1X_2}} = (X_1+X_2)\cdot Q_1 + X_1X_2 = X_1Q_1 + X_2Q_1 + X_1X_2$$

$$Q_2^+ = \overline{\overline{\overline{X}_1X_2\cdot Q_2}\cdot\overline{X_1\overline{X}_2}} = (X_1+\overline{X}_2)\cdot Q_2 + X_1\overline{X}_2 = X_1Q_1 + \overline{X}_2Q_2 + X_1\overline{X}_2$$

$$Z = (Q_1+Q_2)\cdot\overline{Q_1Q_2} = \overline{Q}_1\overline{Q}_2 + Q_1Q_2$$

Q_1Q_2 \ X_1X_2	00	01	11	10
00	00	00	10	01
01	01	00	11	01
11	01	10	11	11
10	00	10	10	11

$Q_1^+ Q_2^+$

Q_1Q_2 \ X_1X_2	00	01	11	10
00	1	1	0	0
01	0	1	1	0
11	0	0	1	1
10	1	0	0	1

Z

SO, THE OUTPUT SEQUENCE = 1 0 1 0 0 1 0 1 1

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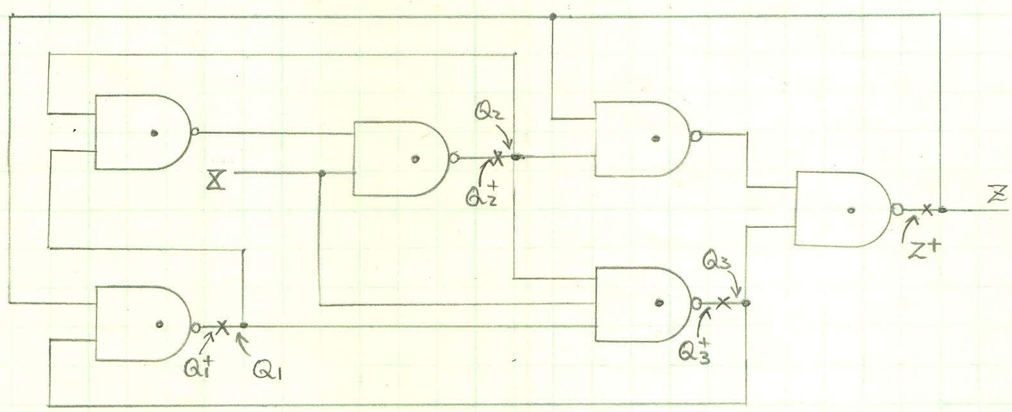
23.4. a. Analyze the following asynchronous network using a flow table. Starting in the stable total state for which $X = Z = 0$, determine the state and output sequences when the input sequence is $X = 0, 1, 0, 1, \cdots$

b. Find any critical races which are present in the table.



---

a. Assign the state variable as above in the figure, we have

$$Q_1^+ = \overline{Z \cdot Q_3} = \bar{Z} + \bar{Q}_3$$

$$Q_2^+ = \overline{X \cdot \overline{Q_1 Q_2}} = \bar{X} + Q_1 Q_2$$

$$Q_3^+ = \overline{X \cdot Q_1 \cdot Q_2} = \bar{X} + \bar{Q}_1 + \bar{Q}_2$$

$$Z^+ = \overline{\overline{Z Q_2} \cdot Q_3} = \bar{Q}_3 + Q_2 Z$$

Then, the flow table is to be on next pages.

Analysis table :

X	Z	Q_1	Q_2	Q_3	Z^+	Q_1^+	Q_2^+	Q_3^+	
0	0	0	0	0	1	1	1	1	
0	0	0	0	1	0	1	1	1	
0	0	0	1	0	1	1	1	1	
0	0	0	1	1	0	1	1	1	
0	0	1	0	0	1	1	1	1	
0	0	1	0	1	0	1	1	1	
0	0	1	1	0	1	1	1	1	
0	0	1	1	1	0	1	1	1	✓
0	1	0	0	0	1	1	1	1	
0	1	0	0	1	0	0	1	1	
0	1	0	1	0	1	1	1	1	
0	1	0	1	1	1	0	1	1	✓
0	1	1	0	0	1	1	1	1	
0	1	1	0	1	0	0	1	1	
0	1	1	1	0	1	1	1	1	
0	1	1	1	1	1	0	1	1	
1	0	0	0	0	1	1	0	1	
1	0	0	0	1	0	1	0	1	
1	0	0	1	0	1	1	0	1	
1	0	0	1	1	0	1	0	1	
1	0	1	0	0	1	1	0	1	
1	0	1	0	1	0	1	0	1	✓
1	0	1	1	0	1	1	1	0	
1	0	1	1	1	0	1	1	0	
1	1	0	0	0	1	1	0	1	
1	1	0	0	1	0	0	0	1	
1	1	0	1	0	1	1	0	1	
1	1	0	1	1	1	0	0	1	
1	1	1	0	0	1	1	0	1	
1	1	1	0	1	0	0	0	1	
1	1	1	1	0	1	1	1	0	✓
1	1	1	1	1	1	0	1	0	

The flow table :

$Z\,Q_1Q_2Q_3$ \ X	$X=0$	$X=1$
0000	1111	1101
0001	0111	0101
0010	1111	1101
0011	0111	0101
0100	1111	1101
0101	0111	0101
0110	1111	1110
0111	0111	0110
1000	1111	1101
1001	0011	0001
1010	1111	1101
1011	0011	1001
1100	1111	1101
1101	0011	0001
1110	1111	1110
1111	1011	1010

$Z^+\ Q_1^+\ Q_2^+\ Q_3^+$

✓

SO, $X = 0, 1, 0, 1, \ldots$

THE OUTPUT $Z = 0\ (0)(0)\ 1\ (1)\ (1)\ 1\ (1)\ (1)\ (0)\ 0\ \ldots$

OR $Z = 0, 1, 1, 0, \ldots$

b.

IF Q_2 CHANGE FIRST

$Z\,Q_1Q_2Q_3$	$X=0$	$X=1$
0 0 0 0	1111	1101
0 0 0 1	0111	0101
0 0 1 0	1111	1101
0 0 1 1	0111	0101
0 1 0 0	1111	1101
0 1 0 1	0111	$\boxed{0101}$
0 1 1 0	1111	1110
0 1 1 1	$\boxed{0111}$	0110
1 0 0 0	1111	1101
1 0 0 1	0011	0001
1 0 1 0	1111	1101
1 0 1 1	$\boxed{1011}$	1001
1 1 0 0	1111	1101
1 1 0 1	0011	0001
1 1 1 0	1111	$\boxed{1110}$
1 1 1 1	1011	1010

$Z^+\ Q_1^+\ Q_2^+\ Q_3^+$

IF Q_1Q_2 CHANGE AT SAME TIME BUT BEFORE Z AND Q_3

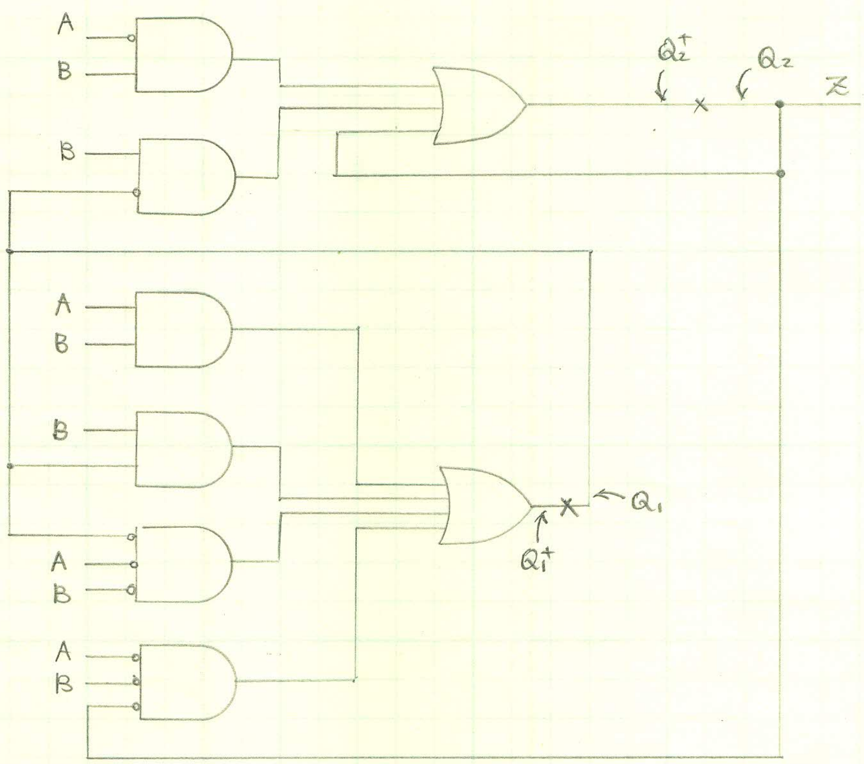
IF Q_2Q_3 CHANGE AT SAME TIME BUT BEFORE Z AND Q_1

?

ANY OTHER CASES WILL STAY IN THIS STABLE STATE FINALLY.

10

Find all critical races and cycles in following circuit.



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SOLUTION: Assign Q_1 & Q_2 as those in the figure above. And then

$$Q_1^+ = AB + BQ_1 + \bar{Q}_1\bar{A}\bar{B} + \bar{A}\bar{B}\bar{Q}_2$$

$$Q_2^+ = A\bar{B} + B\bar{Q}_1 + Q_2$$

$$Z = Q_2$$

A	B	Q_1	Q_2	Q_1^+	Q_2^+	Z
0	0	0	0	1	0	0
0	0	0	1	1	1	1
0	0	1	0	1	0	0
0	0	1	1	0	1	1
0	1	0	0	0	1	0
0	1	0	1	0	1	1
0	1	1	0	1	0	0
0	1	1	1	1	1	1
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	1	1	0
1	1	0	1	1	1	1
1	1	1	0	1	0	0
1	1	1	1	1	1	1

The flow table:

Q_1Q_2 \ AB	00	01	11	10
00	10	01	11	01
01	11	01	11	01
11	01	11	11	01
10	10	10	10	01

Q_2 change first

Q_1 change fast

Q_1Q_2 change at same time

cycle

Now we are going to find the critical races and cycles.

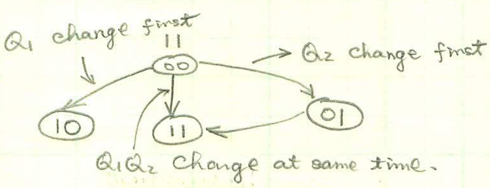
(1) For state $ABQ_1Q_2 = 0000$

non-critical.

(2) For $ABQ_1Q_2 = 0001$

non-critical

(3) $ABQ_1Q_2 = 1100$

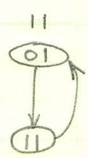


critical race.

(4) $ABQ_1Q_2 = 1000$

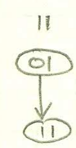
non-critical

(5) $ABQ_1Q_2 = 0001$



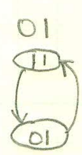
cycle.

(6) $ABQ_1Q_2 = 1101$



non-critical race.

(7) $ABQ_1Q_2 = 0011$

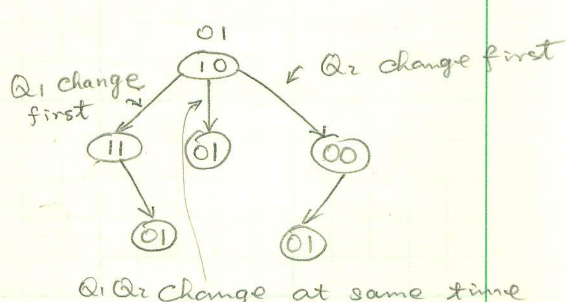


cycle

(8) $ABQ_1Q_2 = 1011$

non-critical

(9) $ABQ_1Q_2 = 1010$



noncritical race.

PROBLEM 24.5 (CONT.)

10

Equivalent states: (5, 14), (1, 9, 12), (2, 11), (4, 13), (10, 15)

Reduced flow table:

X_1X_2 00	01	11	10	Z_1Z_2 00	01	11	10
1	2	4	10	01	—	—	—
5	2	—	3	—	11	—	—
5	2	4	3	—	—	—	11
1	—	4	10	—	—	00	—
5	—	8	—	10	—	—	—
5	6	—	10	—	11	—	—
7	6	8	3	01	—	—	—
7	—	8	3	—	—	00	—
1	6	4	10	—	—	—	11

Reduction by row merger

	X_1X_2 00	01	11	10	Z_1Z_2 00	01	11	10
a, 1	1	2	4	10	01	—	—	—
b, 2,3	5	2	4	3	—	11	—	11
c, 4,10	1	6	4	10	—	—	00	11
d, 5,6	5	6	8	10	10	11	—	—
e, 7,8	7	6	8	3	01	—	00	—

OR.

	X_1X_2 00	01	11	10	Z_1Z_2 00	01	11	10
a 1,4	1	2	4	10	01	—	00	—
b 2,3	5	2	4	3	—	11	—	11
c 5,6	5	6	8	10	10	11	—	—
d 7,8	7	6	8	3	01	—	00	—
e 10	1	6	4	10	—	—	—	11

The minimum-row flow table is not unique.

24.5 For the following primitive flow table, find the equivalent stable total states and reduce the table accordingly. Complete the reduction by row merger and then derive a corresponding output table. Is the minimum-row flow table unique?

X_1X_2 00	01	11	10	Z_1Z_2
1	11	4	10	01
5	2	–	3	11
5	2	13	3	11
12	–	4	15	00
5	–	8	–	10
14	6	–	10	11
7	6	8	3	01
7	–	8	3	00
9	11	13	10	01
12	6	13	10	11
5	11	–	3	11
12	2	4	15	01
1	–	13	10	00
14	–	8	–	10
1	6	4	15	11

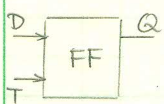
SOLUTION: Potentially equivalent stable total states:

(5, 14), (1, 7, 9, 12), (2, 6, 11), (4, 8, 13), (3, 10, 15)

1-7	11-6 , 10~10 .	X
1-9	~~11~11~~ , 4 ~ 13, ~~10~10~~	✓
1-12	~~11~2, 4~4~~ , 10~15	✓
7-9	6 ~ 11 , 10 ~ 10	X
7-12	6 ~ 2 , 8 ~ 4 , 3 ~ 15	X
9-12	~~11~2~~ , 13~4 , 10~15	✓
2-6	5 ~ 14 , 3 ~ 10	X
2-11	5 ~ 5 , 3 ~ 3	✓
6-11	14 ~ 5 , 10 ~ 3	X
4-8	12 ~ 7 , 15 ~ 3	X
4-13	12 ~ 1 , 15 ~ 10	✓
8-13	7 - 1 , 3 ~ 10	X
3-10	5 ~ 12, 2 - 6 , 13 ~ 13	X
3-15	5 ~ 1 , 2 ~ 6 , 13 ~ 4	X
10-15	12 ~ 1 , ~~6~6~~ , 13 ~ 4	✓
5-14	8 ~ 8	✓

24.6 One type of clocked D-flip-flop works as follows:

On the trailing edge of the clock pulse (1 to 0 transition) the output Q assumes the same state which the input D had on the leading edge of the clock pulse (0 to 1 transition). The output does not change at any other time. D may change at any time with respect to the clock. When D changes simultaneously with the leading edge of the clock, the value D had immediately before the change should determine the output after the clock pulse. Find a minimum-row flow table.



		DT 00	01	11	10	Q
(DT=00)	1	1	2	4	3	0
(DT=01)	2	1	2	4	7	0
(DT=10)	3	1	6	4	3	0
(DT=11)	4	1	2	4	7	0
(DT=00)	5	5	6	4	7	1
(DT=01)	6	1	6	8	7	1
(DT=10)	7	5	6	8	7	1
(DT=11)	8	1	6	8	7	1

The minimum-row flow table:

	DT 00	01	11	10	Q
1	1	2	4	3	0
2,4	1	2	4	7	0
3	1	6	4	3	0
5	5	6	4	7	1
6,8	1	6	8	7	1
7	5	6	8	7	1

OK

Dr. Allwine, I don't understand why the solution in text has the same stable states on the same rows. I can't find such an example in Chapter 24.

They merged ~~[illegible]~~ three rows into row 1 & then renamed them all 1. etc for other merged rows.

10

25.2 Make a proper assignment of internal state variable for each of the following flow tables. In each case, 3 internal state variables are sufficient. Specify the final state tables in term of interms of internal states.

(a)

X_1X_2	00	01	11	10
a	1	4	7	10
b	1	5	8	11
c	2	6	8	10
d	2	4	9	11
e	3	6	9	10
f	3	5	7	12

(b)

X_1X_2	00	01	11	10
a	1	4	7	11
b	2	6	8	10
c	3	6	7	10
d	2	4	9	10
e	1	5	9	10
f	3	6	7	11
g	2	6	9	11
h	1	5	7	11

SOLUTION: (a) Required Transitions:

COLUMN 00 : $b \to a$, $c \to d$, $e \to f$

COLUMN 01 : $a \to d$, $e \to c$, $f \to b$

COLUMN 11 : $f \to a$, $c \to b$, $d \to e$

COLUMN 10 : $a \to c$, $e \to c$, $b \to d$

Using Shared Row Assignments:

column 00: (a, b)✓, (c, d)✓, (e, f)✓

column 01: (a, d)✓, (c, e)✓, (b, f)✓

column 11: (a, f)✓, (b, c)✓, (d, e)✓

column 10: (a, e)✓, ~~(c, e)~~, (b, d)✓

Assign:

a	c
f	e

Statisfy: (a, c), (a, f), (c, e), (e, f)

Then

a	c
α	β
b	d
f	e

X_1X_2	00	01	11	10
a	1	α	7	10
b	α	5	8	11
c	β	6	β	10
d	2	4	9	11
e	3	6	9	10
f	3	5	7	12
α	1	β	8	—
β	2	4	α	—

(b) Required transitions:

COLUMN 00 : $e \to a$, $h \to a$, $d \to b$, $g \to b$, $f \to c$.

COLUMN 01 : $a \to d$, $b \to f$, $c \to f$, $g \to f$, $h \to e$

COLUMN 11 : $c \to a$, $f \to a$, $h \to a$, $d \to g$, $e \to g$.

COLUMN 10 : $a \to h$, $f \to h$, $g \to h$, $d \to c$, $e \to c$, $b \to c$

Using Shared Row Assignments.

COLUMN 00 : (a, e, h) (b, d, g) (f, c)

COLUMN 01 : (a, d) (b, c, f, g) (e, h)

COLUMN 11 : (a, c, f, h) (d, e, g)

COLUMN 10 : (a, f, g, h) (b, c, d, e)

Assign

a	h
f	c
d	e

Statisfy : (a, d) , (f, c) , (e, h) , (a, e, h)

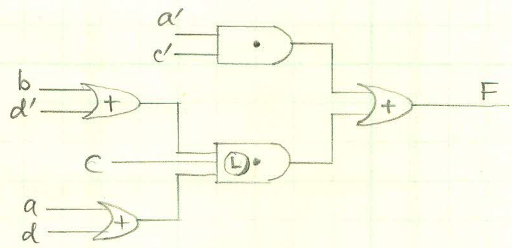
Then

a	h
f	c
g	b
d	e

Statisfy : (b, d, g) , (b, c, f, g) , (a, c, f, h)

(d, e, g) , (a, f, g, h) , (b, c, d, e)

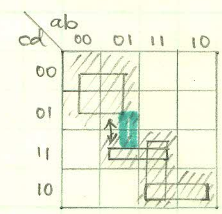
26.1 Find all of the static hazards in the following network. For each hazard, specify the values of the variables which are constant and the variable which is changing. Indicate how all of these hazards could be eliminated by adding gates to the existing network. (This means that you can add gates or gate input to the network as it stands, but you cannot change any of the connections in the given network.)



SOLUTION: $F^t = a'c' + (b+d')\cdot c\cdot(a+d)$.

$= a'c' + abc + bcd + acd' + cdd'$

K-map:



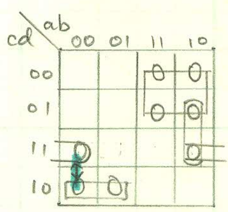
from the map, we can see that there is an 1-hazard between

abcd = 0101 and 0111, only c is changing.

We can add $a'bd$ term at input of the rightmost OR gate to eliminate the one hazard.

$F^{t'} = (a+c)\cdot[c' + a'd' + b'd] = ac' + aa'd' + ab'd + cc' + a'cd' + b'cd$

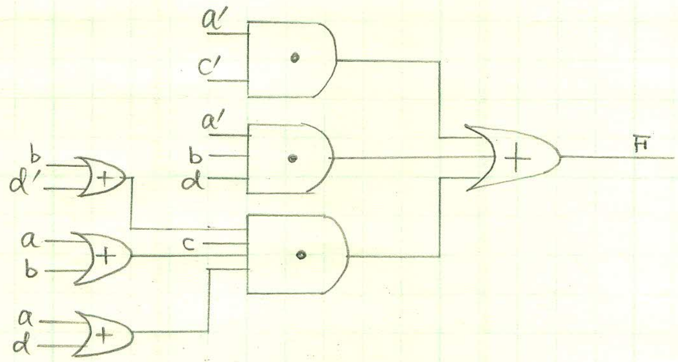
K-map:



A zero hazard between 0010 and 0011, only d is changing.

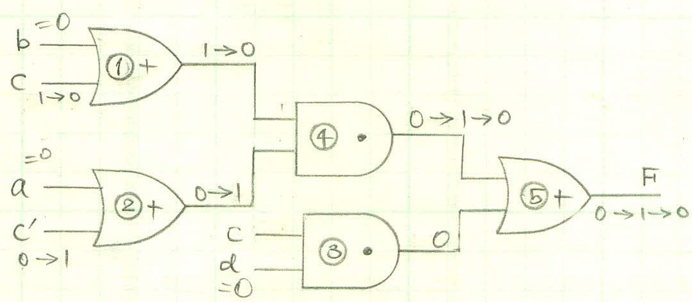
And adding a+b term at gate L will eliminate the zero hazard.

<u>The following is the static hazards free for Problem 26.1</u>:



END OF 26.1

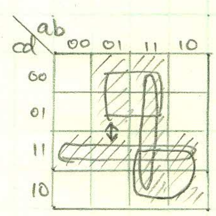
26.2 a. Find all of the static hazards in the following network. For each hazard, specify the values of input variables and which variable is changing when hazard occurs. Also specify the order in which the gate outputs must change.



<u>Solution:</u> $F^t = (a+c')(b+c) + cd = ab + ac + c'b + c'c + cd$

$$F^{t'} = (c'+d')\cdot(b'c'+a'c) = a'cc' + a'cd' + b'c'd' + b'c'$$

K-map for F^t:

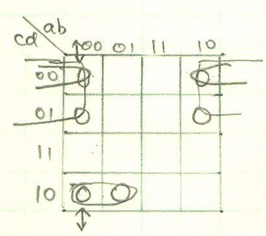


From map, we have 1-hazard between 0101 ↔ 0111 only c is changing.

Gate change for c: 0→1 : ② ④ ⑤ ③ ⑤.

Gate changes for c: 1→0 : ③ ⑤ ② ④ ⑤

K-map for: $F^{t'} \to F^t$

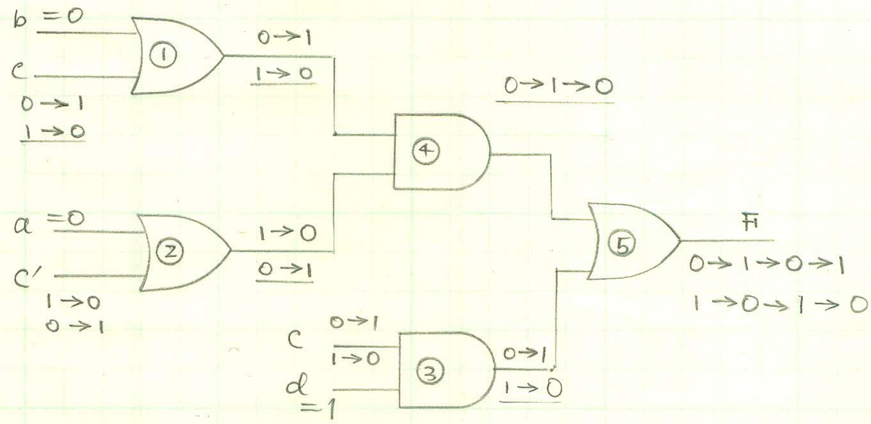


From map, we have 0-hazard between 0000 ↔ 0010 ; only c is changing.

Gate changes for c: 0→1: ① ④ ⑤ ② ④ ⑤

Gate changes for c: 1→0: ② ④ ⑤ ① ④ ⑤

b. There is a dynmic hazard which occurs when the output of the network changes from 0 to 1. Specify the values of the input variables before and after. In which order must the gate outputs switch in order for this hazard to occur?



<u>Solution:</u> Inspection of the network shows that the only input variable which could cause a dynamic hazard when it changes is C.

Let $a = b = 0$, $d = 1$

If $C: 0 \to 1$, then the gate outputs:

1 4 5 2 4 5 3 5.

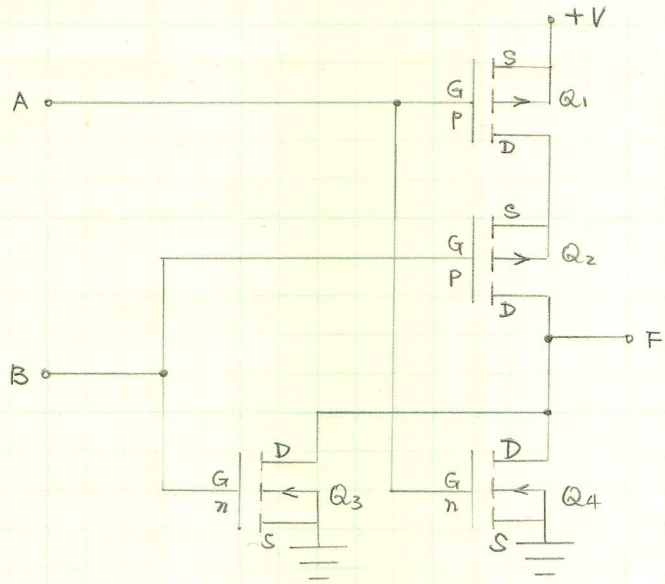
If $C: 1 \to 0$, then the gate outputs:

3 5 2 4 5 1 4 5

10

A.4 For the following CMOS network, make a table similar to Fig A-15 (b).

What type of CMOS gate is this?



Solution: The truth table

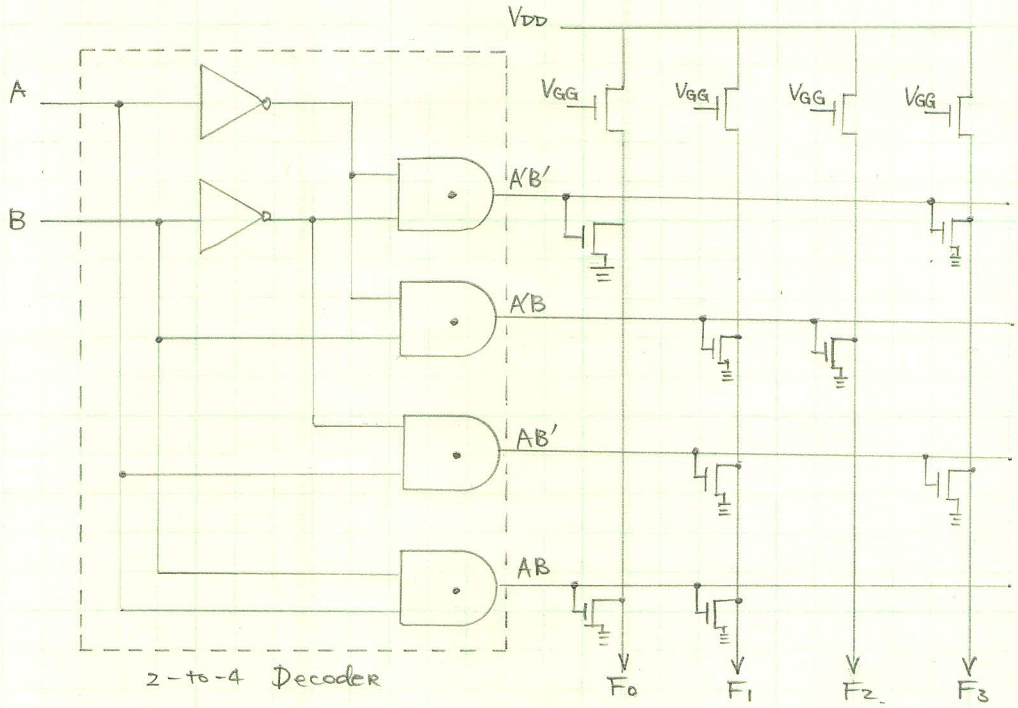
A	B	F	Q_1	Q_2	Q_3	Q_4
0	0	+V	ON	ON	OFF	OFF
0	+V	0	ON	OFF	ON	OFF
+V	0	0	OFF	ON	OFF	ON
+V	+V	0	OFF	OFF	ON	ON

$F = \overline{(A+B)}$, So, the cercuit is CMOS NOR.

Self-notes: $V_G = 0$: type p → ON type n → OFF

$V_G = 1$: type P → OFF type n → ON.

A.5. MOSFETs can be connected in a regular pattern to form the memory array for a read-only (see Fig. 9-21) or a programmed logic array (see Fig. 9-25). For the 4 word × 4 bit read-only memory shown below, determin the four output functions realized by the MOS array.



Solution:

A	B	F_0	F_1	F_2	F_3
0	0	0	1 (V_{DD})	1 (V_{DD})	0
0	1	1 (V_{DD})	0	0	1 (V_{DD})
1	0	1 (V_{DD})	0	1 (V_{DD})	0
1	1	0	0	1 (V_{DD})	1 (V_{DD})

F_0:

B \ A	0	1
0	0	1
1	1	0

F_1:

B \ A	0	1
0	1	0
1	0	0

F_2:

B \ A	0	1
0	1	1
1	0	1

F_3:

B \ A	0	1
0	0	0
1	1	1

$F_0 = AB' + A'B = A \oplus B$ ✓ $\quad F_1 = A'B'$ ✓

$F_2 = A + B'$ ✓ $\quad F_3 = B$ ✓

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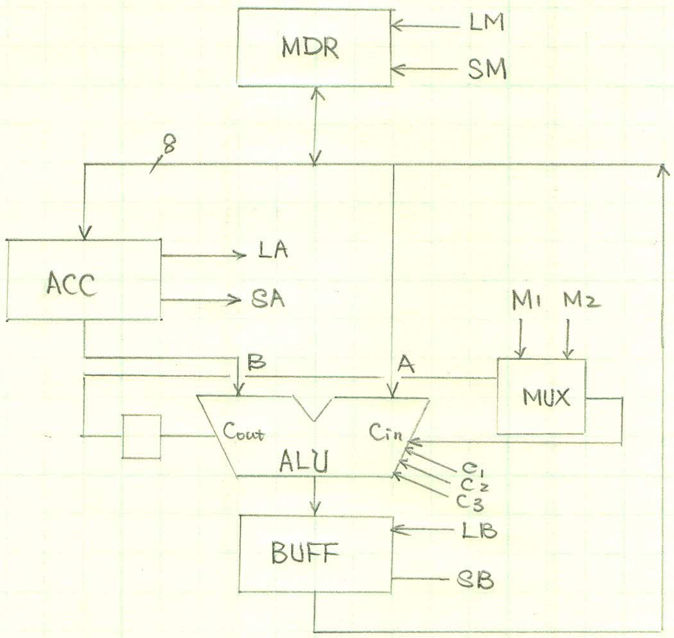

	C_1	C_2	C_3	M_1	M_2	LA	SA	LB	SB	LM	SM
MDR → ACC	X	X	X	X	X	1	0	0	0	0	1
ADR+ACC → ACC	0	0	0	0	0	0	1	1	0	0	1
	X	X	X	X	X	1	0	0	1	0	0
Comp ACC → ACC	0	1	1	0	0	0	1	1	0	0	0
	X	X	X	X	X	1	0	0	1	0	0

#