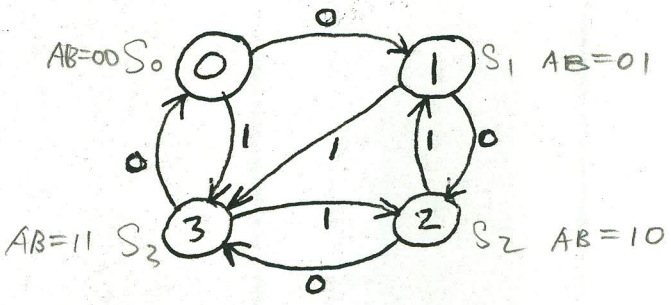
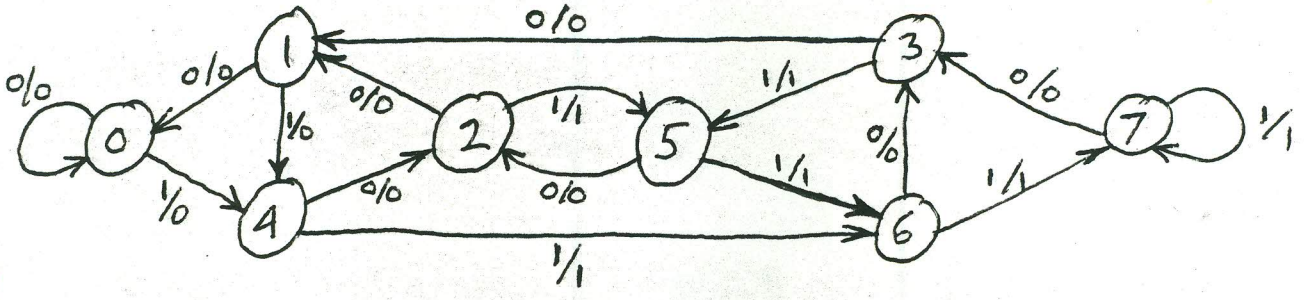
EE 410 EXAM #1 CLOSED BOOK AUT. 1987 Benmei Chen

(One sheet of notes permitted -- attach to exam paper)

1. Write J-K flip-flop input equations for this sequential machine:



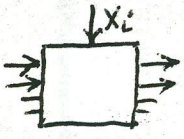
2. Redraw this state graph with all redundant states removed (if any):



3. Design a typical cell for a space iterative network to detect a legal 2-out-of-5 code.

(A 2-out-of-5 code contains two ones and three zeros)

Five of these cells are to be used, each with a one bit input plus a necessary number of lines to propagate state information between cells.



A termination cell is also required which will produce $Z=1$ for a legal code and $Z=0$ for an illegal code.

Show a typical iterative cell, the termination cell, and how to connect the complete system.

1. FLIP-FLOPS:

(1) J-K FLIP-FLOP:

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$Q^+ = JQ' + K'Q$

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

(2) D FLIP-FLOP

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

$Q^+ = D$

(3) T FLIP-FLOP

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

$Q^+ = T \oplus Q$

(4) S-R FLIP-FLOP

S	R	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	–
1	1	1	–

} not allowed

$Q^+ = S + R'Q$

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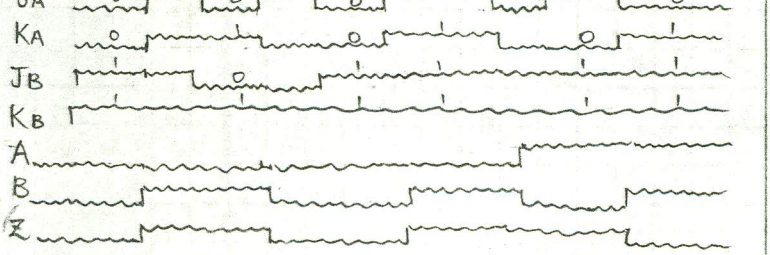
2. EXAMPLE FOR DRAWING THE TIMING CHART:

FROM STATE GRAPH, ASSIGN FF #, AND TO EACH STATE, CREATE STATE TABLE. e.g.

X	A	B	A^+	B^+	J_A	K_A	J_B	K_B	Z
0	0	0	0	1	0	X	1	X	1
0	0	1	1	0	1	X	X	1	1
0	1	0	1	1	X	0	1	X	0
0	1	1	0	0	X	1	X	1	0
1	0	0	1	0	1	X	0	X	1
1	0	1	0	0	0	X	X	1	0
1	1	0	1	1	X	0	1	X	1
1	1	1	0	0	X	1	X	1	0

⇒ KARNAUGH MAP: $J_A = X'B + XB'$, $K_A = B$, $J_B = X' + A$, $K_B = 1$, $Z = (A^+)'B^+ + A^+(B^+)'$



* MOORE NO FULSE OUTPUT, MEALY MAY HAVE.

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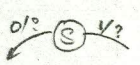
3. DEFERENCES BETWEEN MOORE & MEALY STATE GRAGH & TABLE:

MOORE: 

MEALY 

PRE. S.	NEXT X=0, X=1	Z

,

P.STATE	NEXT X=0 X=1	OUTPUT X=0 X=1

---

4. Guideline for STATE ASSIGNMENT: (BY EXAMPLE)

	X=0	1	0 1
S_0	S_1	S_2	0 0
S_1	S_3	S_2	0 0
S_2	S_1	S_4	0 0
S_3	S_5	S_2	0 0
S_4	S_1	S_6	0 0
S_5	S_5	S_2	1 0
S_6	S_1	S_6	0 1

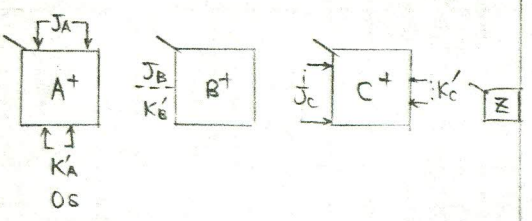
G.1. (S_0, S_1, S_3, S_5) (S_3, S_5) (S_4, S_6) (S_0, S_2, S_4, S_6)

2. (S_1, S_2) (S_2, S_3) (S_1, S_4) (S_2, S_5) 2X (S_1, S_6) 2X

BC \ A	0	1
	S_0	
	S_2	S_5
	S_4	S_2
	S_6	S_1

STATE MAP

BC \ XA				
	S_1	X	X	S_2
	S_1	S_5	S_2	S_4
	S_1	S_5	S_2	S_6
	S_1	S_3	S_2	S_6



OS

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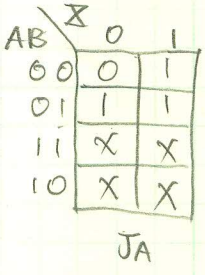
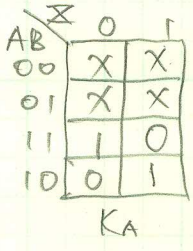
5. LOGIC ELEMENTS

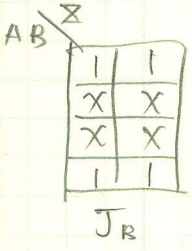
"AND"  "OR"   "INVERSE"

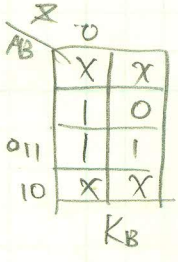
1. TWO J-K F.F NEEDED FOR THIS MECHINE:

X A B	A^+ B^+	J_A K_A	J_B K_B
0 0 0	0 1	0 X	1 X
0 0 1	1 0	1 X	X 1
0 1 0	1 1	X 0	1 X
0 1 1	0 0	X 1	X 1
1 0 0	1 1	1 X	1 X
1 0 1	1 1	1 X	X 0
1 1 0	0 1	X 1	1 X
1 1 1	1 0	X 0	X 1









$J_A = \bar{X} + B$ ✓ $K_A = X\bar{B} + B\bar{X}$ ✓ $J_B = 1$ ✓ $K_B = \bar{X} + A$ ✓

2.

STATE	NEXT X=0	NEXT X=1	OUTPUT X=0	OUTPUT X=1
✓ S_0	S_0	S_4	0	0
~~S_1~~	S_0	S_4	0	0
✓ S_2	~~$S_1 S_0$~~	~~$S_5 S_4$~~	0	1
~~S_3~~	~~$S_1 S_0$~~	~~S_5~~	0	1
✓ S_4	S_2	$S_6 S_4$	0	1
~~S_5~~	S_2	S_6	0	1
~~S_6~~	~~$S_3 S_2$~~	~~$S_7 S_6$~~	0	1
~~S_7~~	S_3	S_7	0	1

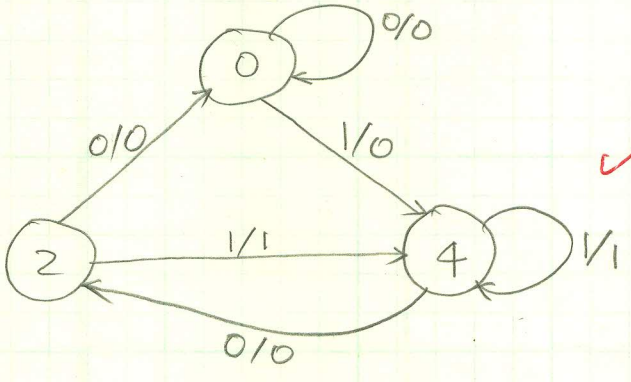
$S_1 = S_0$

$S_3 = S_2$

$S_6 = S_5 = S_4$

$S_7 = S_6$

answer:



✓

3. I THINK WE HAVE TO USE FOUR STATES TO "REMEMBER"

INPUTS FROM LEFT-HAND SIDE HAVE

S_0 ⇒ ZERO 1's, S_1 = one 1, S_2 = Two 1's S_3 > TWO 1's
AB = 00 AB = 01 AB = 10 AB = 11

FOR TYPICAL CELL i ~~(WE ARE GOING TO USE TWO D-F.F.)~~

S_i	S_{i+1} $X_i=0$	$X_i=1$	Z
S_0	S_0	S_1	0
S_1	S_1	S_2	0
S_2	S_2	S_3	1
S_3	S_3	S_3	0

A_i B_i	A_{i+1} B_{i+1} $X_i=0$	$X_i=1$	Z
0 0	0 0	0 1	0
0 1	0 1	1 0	0
1 0	1 0	1 1	1
1 1	1 1	1 1	0

A_iB_i \ X_i	0	1
00	0	0
01	0	1
11	1	1
10	1	1

A_{i+1}

A_iB_i \ X_i	0	1
00	0	1
01	1	0
11	1	1
10	0	1

B_{i+1}

B_i \ A_i	0	1
0	0	1
1	0	0

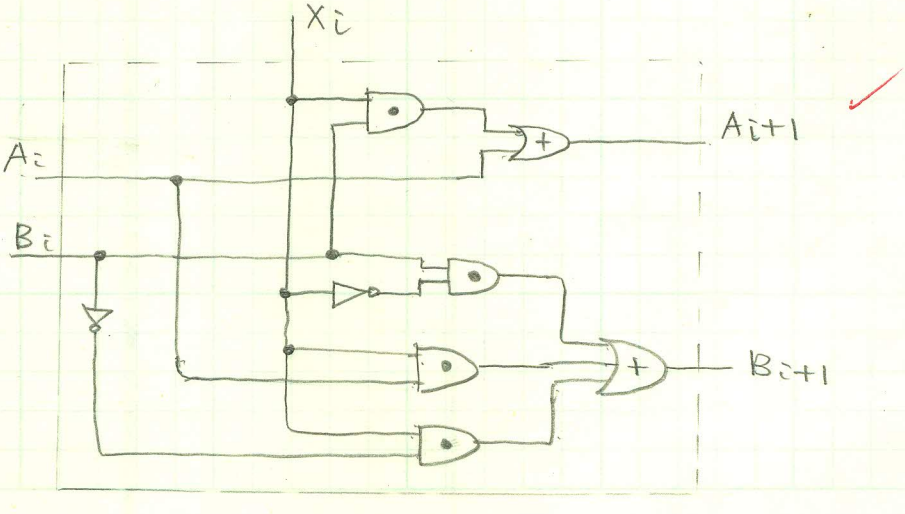
Z

$A_{i+1} = A_i + B_i X_i$ ✓

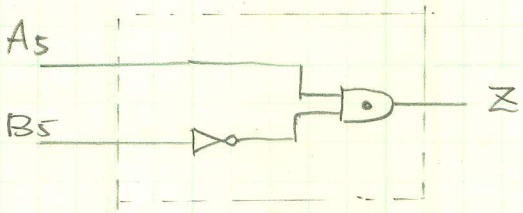
$B_{i+1} = B_i \bar{X}_i + A_i X_i + \bar{B}_i X_i$ ✓

$Z = A_i \bar{B}_i$ ✓

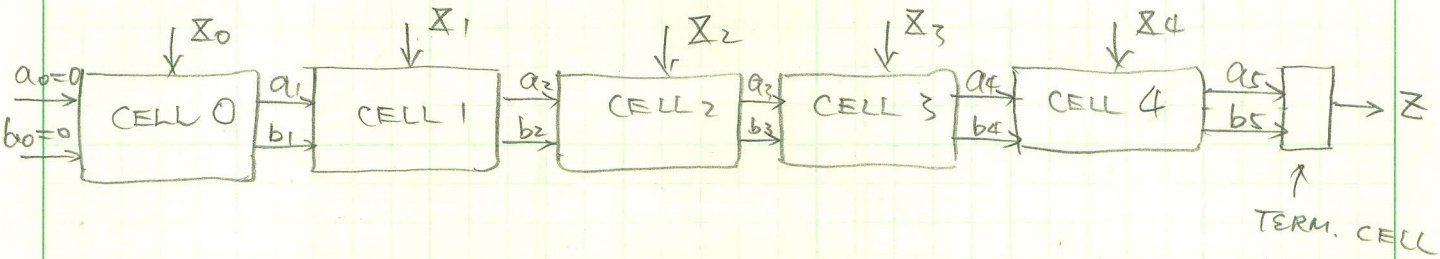
THE TYPICAL CELL CIRCUIT:



TERMINATION CELL



③ CONNECTION



$a_i = A_i$
$b_i = B_i$

Good

C	H	E	N

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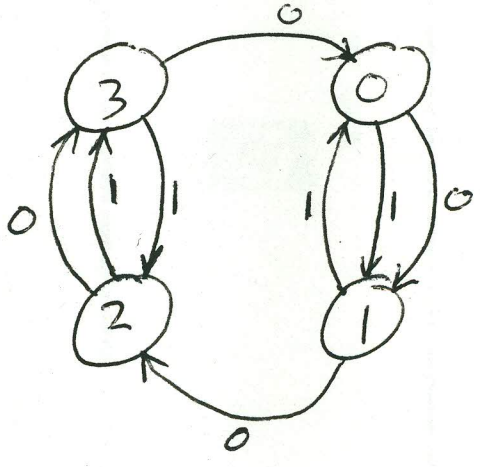
EE 410 EXAM #2

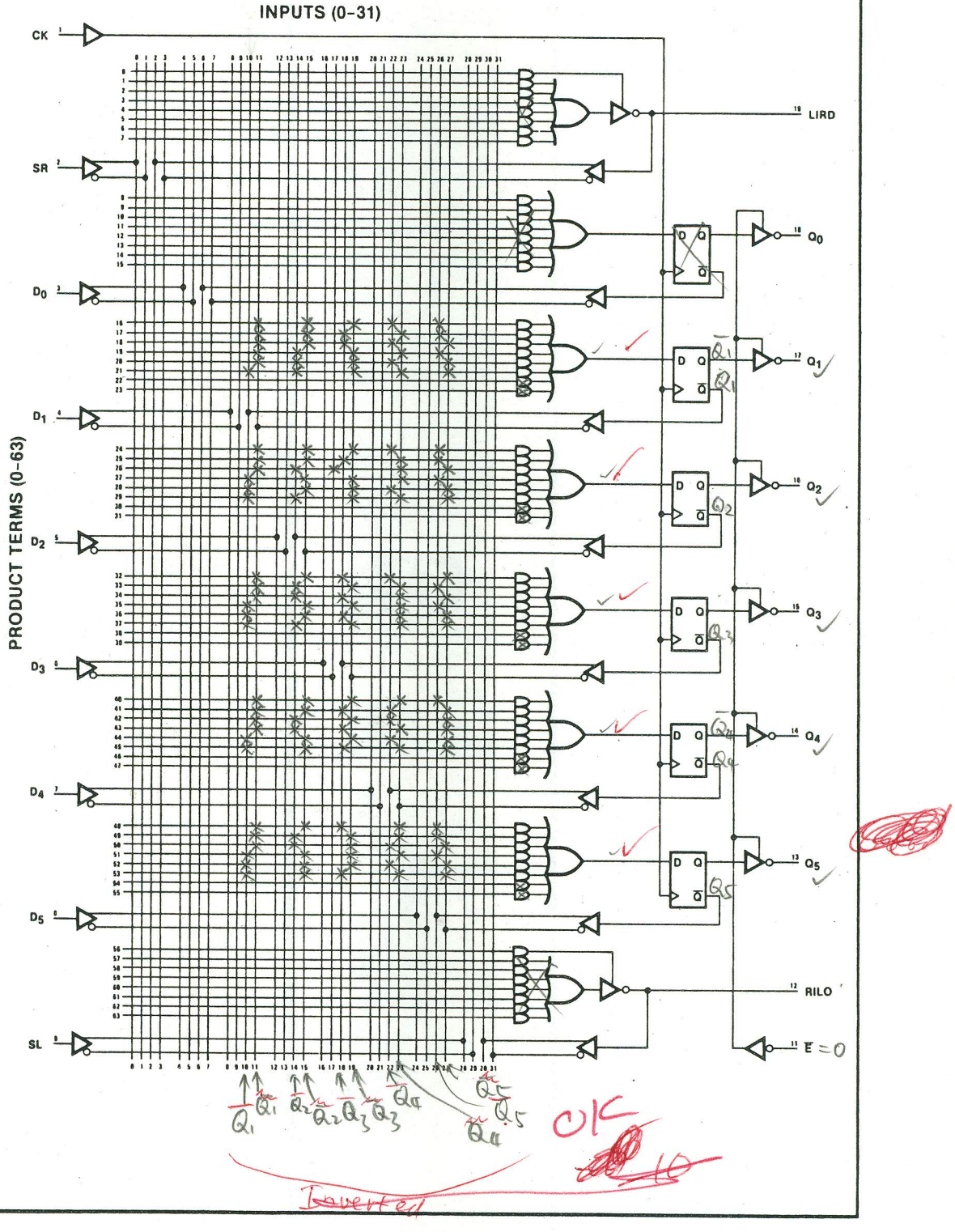
ONE SHEET OF NOTES & OPEN BOOK

1. Use a PAL16R6 to design a "2-out-of 5" code up-counter (see page 13 for code sequence). Show your design on the PAL diagram sheet attached. Take into account the fact that the PAL outputs are inverted.

2. Use a 74163 counter to build this state machine. Show a complete circuit



Logic Diagram PAL16R6



PROBLEM 1: USE PAL16 R6 TO BUILD A up-COUNTER FOR "2-out-of-5" code

INPUT					OUTPUT									
Q_1	Q_2	Q_3	Q_4	Q_5	Q_1^+	Q_2^+	Q_3^+	Q_4^+	Q_5^+	D_1	D_2	D_3	D_4	D_5
0	0	0	1	1	0	0	1	0	1	1	1	0	1	0
0	0	1	0	1	0	0	1	1	0	1	1	0	0	1
0	0	1	1	0	0	1	0	0	1	1	0	1	1	0
0	1	0	0	1	0	1	0	1	0	1	0	1	0	1
0	1	0	1	0	0	1	1	0	0	1	0	0	1	1
0	1	1	0	0	1	0	0	0	1	0	1	1	1	0
1	0	0	0	1	1	0	0	1	0	0	1	1	0	1
1	0	0	1	0	1	0	1	0	0	0	1	0	1	1
1	0	1	0	0	1	1	0	0	0	0	0	1	1	1
1	1	0	0	0	0	0	0	1	1	1	1	1	0	0

$$D_1 = \bar{Q}_1 \bar{Q}_2 \bar{Q}_3 Q_4 Q_5$$

$$+ \cdots$$

DONE IN CIRCUIT attached !

PROBLEM 2: STATE TABLE:

	PRE.	NEXT $x=0$	NEXT $x=1$
0 0	S_0	S_1	S_1
0 1	S_1	S_2	S_0
1 0	S_2	S_3	S_3
1 1	S_3	S_0	S_2

Q_B Q_A	$x=0$ Q_B^+	Q_A^+	$x=1$ Q_B^+	Q_A^+
0 0	0	1	0	1
0 1	1	0	0	0
1 0	1	1	1	1
1 1	0	0	1	0

x	B	A	B^+	A^+	CLEAR	LOAD	D_B	D_A	PT
0	0	0	0	1	1	1	X	X	1
0	0	1	1	0	1	1	X	X	1
0	1	0	1	1	1	1	X	X	1
0	1	1	0	0	0	X	X	X	X
1	0	0	0	1	1	1	X	X	1
1	0	1	0	0	0	X	X	X	X
1	1	0	1	1	1	1	X	X	1
1	1	1	1	0	1	0	1	0	X

$\therefore$ $D_B = 1$ ✓ $D_A = 0$ ✓ $PT = 1$ ✓ -3

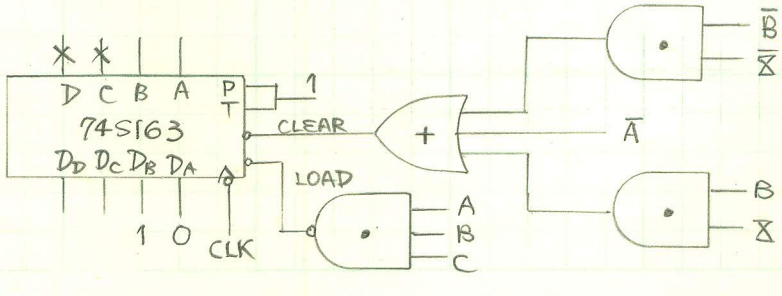
$LOAD = \bar{x} + \bar{B} + \bar{A} = \overline{ABC}$

reduces to $\bar{x} + \bar{A}$

BA \ x	0	1
00	1	1
01	1	0
11	0	1
10	1	1

$CLEAR = \bar{A} + \bar{B}\bar{x} + Bx$ ✓

THE COMPLETE CIRCUIT:



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EE-410 EXAM #3 AUT. 87 OPEN BOOK & ONE SHEET OF NOTES

1. Eliminate all redundant rows in the following primitive flow table, then convert to Mealy and merge all possible rows.

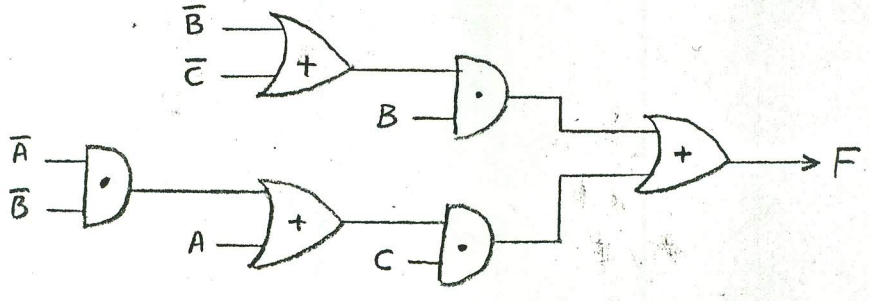
	AB 00	01	11	10	Z
1	(1)	4	2	3	1
2	1	8	(2)	3	1
3	9	8	7	(3)	0
4	1	(4)	7	6	0
5	(5)	4	7	6	1
6	5	4	2	(6)	0
7	9	8	(7)	3	1
8	5	(8)	2	10	0
9	(9)	4	2	3	1
10	1	8	7	(10)	1
11	5	4	(11)	10	1

2. Problem 27D on page 590 has the following primitive flow table

	X1 X2 00	01	11	10	Z
1	(1)	5	-	2	1
2	8	-	3	(2)	1
3	-	4	(3)	7	1
4	1	(4)	6	-	1
5	1	(5)	6	-	0
6	-	4	(6)	7	0
7	8	-	3	(7)	0
8	(8)	5	-	2	0

There are no redundant states, and none merge.
Find a set of race-free state assignments for this problem.
Show the binary bits assigned to each state.

3. Identify all static hazards in the following circuit, and draw an equivalent circuit which is free of static hazards.



1. The following are all the potentially equivalent stable total states: (100)

(1,5), (1,9), (5,9), (4,8), (2,7), (7,11), (2,11), (3,6)

1-5	2-7, 3-6	X
1-9	✓	✓ ✓
5-9	7-2, 6-3	X
4-8	1-5, 7-2, 6-10	X
2-7	1-9	✓ ✓
7-11	9-5, 8-4, 3-10	X
2-11	1-5, 8-4, 3-10	X
3-6	9-5, 8-4, 7-2	X

The equivalent s.t.s are (1,9) and (2-7)

Reduced

	AB 00	01	11	10		z 00	01	11	10
1	①	4	2	3		1	–	–	–
2	1	8	②	3	}	–	–	1	–
3	1	8	2	③		–	–	–	0
4	1	④	2	6		–	0	–	–
5	⑤	4	2	6	}	1	–	–	–
6	5	4	2	⑥		–	–	–	0
8	5	⑧	2	10		–	0	–	–
10	1	8	2	⑩		–	–	–	1
11	5	4	⑪	10		–	–	1	–

Mealy merge

		AB 00	01	11	10		z 00	01	11	10
a	1	①	4	2	3	×	1	–	–	–
b	2, 3	1	8	②	③	×	–	–	1	0
c	4	1	④	2	6	×	–	0	–	–
d	5, 6	⑤	4	2	⑥	×	1	–	–	0
e	8	5	⑧	2	10		–	0	–	–
f	10	1	8	2	⑩	×	–	–	–	1
g	11	5	4	⑪	10		–	–	1	–

OR :

	AB 00	01	11	10	z 00	01	11	10
a	ⓐ	c	b	b	1	–	–	–
b	a	e	ⓑ	ⓑ	–	–	1	0
c	a	ⓒ	b	d	–	0	–	–
d	ⓓ	c	b	ⓓ	1	–	–	0
e	d	ⓔ	b	f	–	0	–	–
f	a	e	b	ⓕ	–	–	–	1
g	d	c	ⓖ	f	–	–	1	–

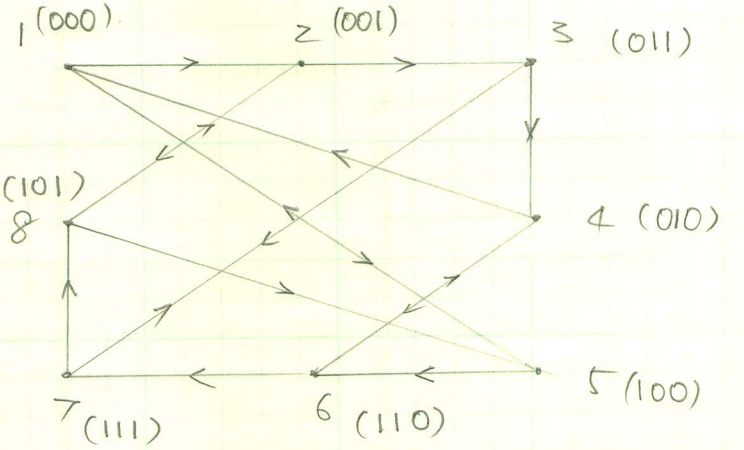
2. Required transition:

col: 00 : 2,7 → 8 , 4,5 → 1

col: 01 : 1,8 → 5 , 3,6 → 4

col: 11 : 2,7 → 3 , 4,5 → 6

col: 10 : 1,8 → 2 , 3,6 → 7



OR

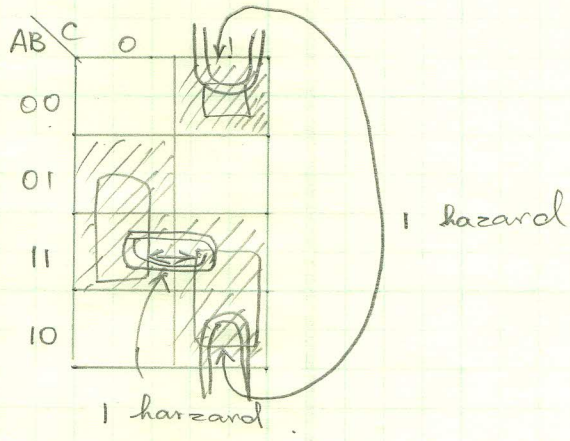
	0	1
00	1	5
01	2	8
11	3	7
10	4	6

✓

3. From the circuit given in test sheet, we have

$$F^t = (\bar{A}\bar{B} + A)C + (\bar{B}+\bar{C})\cdot B$$

$$= \bar{A}\bar{B}C + AC + B\bar{B} + B\bar{C}$$



One-hazards occur at $ABC = 001 \leftrightarrow 101$

and $ABC = 110 \leftrightarrow 111$

To eleminate the one-hazards, we have add two terms to F^t : AB and $\bar{B}C$ ✓

$$(F^t)' = \overline{(\bar{A}\bar{B}+A)C + (\bar{B}+\bar{C})B}$$

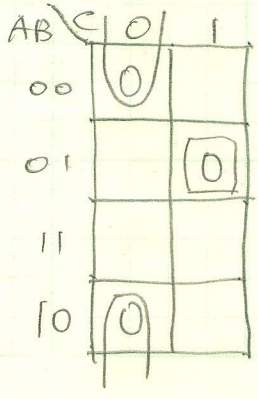
$$= \overline{(\bar{A}\bar{B}+A)C} \cdot \overline{(\bar{B}+\bar{C})B}$$

$$= \left[\overline{(\bar{A}\bar{B}+A)} + \bar{C}\cdot\right]\cdot\left[\overline{(\bar{B}+\bar{C})} + \bar{B}\right]$$

$$= \left[(A+B)\cdot\bar{A} + \bar{C}\right]\cdot\left[BC + \bar{B}\right]$$

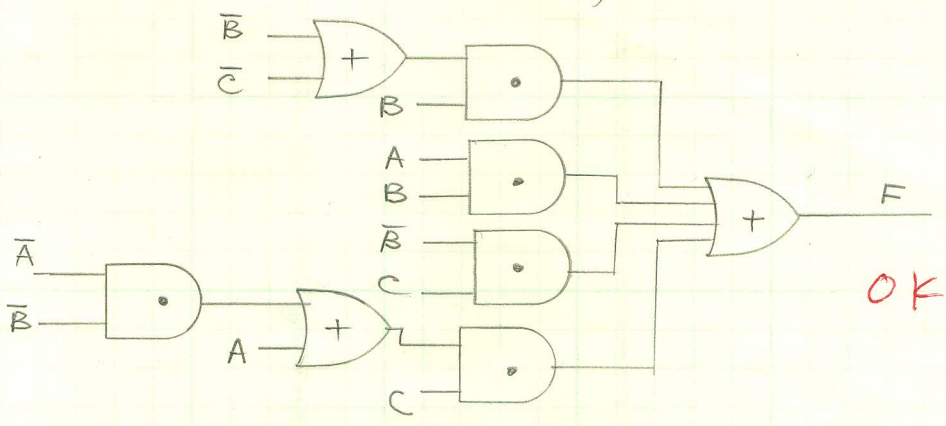
$$= (A\bar{A} + \bar{A}B + \bar{C})(BC + \bar{B})$$

$$= A\bar{A}BC + \bar{A}BBC + BC\bar{C} + A\bar{A}\bar{B} + \bar{A}B\bar{B} + \bar{B}\bar{C}$$



no zoro-hazaral

The equivalent static hazard free circuit:



OK

Benmei Chen

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EE 410 FINAL EXAM Autumn 1987 Open Book

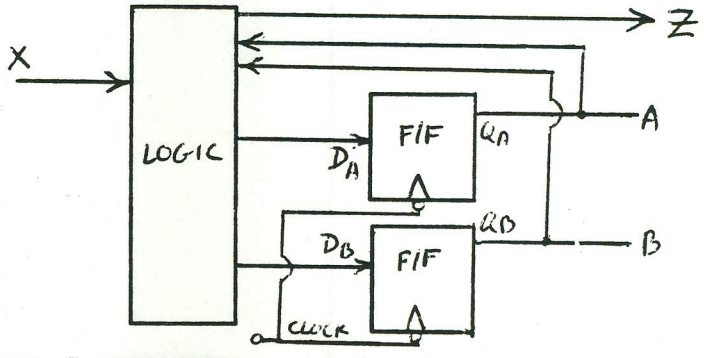
1. What are the outstanding characteristics of :

TTL	ECL
CMOS	I^2L

2. What are three sources of noise in a circuit board layout containing integrated circuits, and what could be done to help eliminate each ?

3. Consider this synchronous machine containing two D-flip-flops and combinational logic.
   a) Is it a Mealy or Moore ?
   b) Draw a state graph.
   c) Draw a timing diagram showing the clock, X, A, B, Z. Assume A=B=0 initially, and the input changes midway between clock pulses. Use the input sequence X = 10011

X	A	B	Da	Db	Z
0	0	0	0	0	0
0	0	1	0	1	1
0	1	x	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	0	0



4. A door lock operates as follows: Inputs XY must be pressed in this sequence to unlock the door: (00), 01, 11, 10, 00. After inputting this sequence, the electric door latch will operate every time X is pressed. If Y is pressed, however, the system resets, and the unlock sequence must be entered to open the door again.
Derive a minimum row flow table for this asynchronous system.

5. Make a set of race-free state assignments for the machine depicted by this flow table. Also, complete the output part of the table.

Present State	Next State 00	01	11	10	Outputs 00	01	11	10	<-- X1,X2
a	(a)	c	(a)	b	01		10		
b	(b)	d	a	(b)	01			00	
c	(c)	(c)	e	b	11	10			
d	a	(d)	g	-		11			
e	-	d	(e)	b			00		
f	b	-	e	(f)				11	
g	-	c	(g)	f			01		

PROBLEM 1:

1. FOR TTL, more capable of driving more gate inputs and faster than diode. And lower power consumption.
2. ECL : fast
3. Compared with TTL, CMOS has the advantage of much lower power dissipation.
4. I^2L, use currents instead of votalges.

PROBLEM 2: THREE NOISE SOURCES:

1. Power and ground distribution problems
2. Signal crosstalk.
3. Transmission-line effects.

1. For the first noise source, it can be minimized by keeping the power and ground lines as shot and as direct as possible. such as to use a grid of conductors that approximates a plane. And the noise problem is solved by the use of capacitors called decoupling.

2. Crosstalk can be reduced by physically separating crosstalk-prone conductors. It also can be reduced by the use of a good ground plane or grid.

3. To match the characteristic impedance of the trasmission line like themselve.

3.

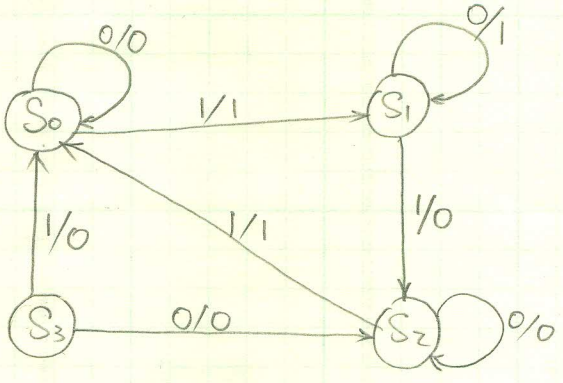
X	A	B	A^+	B^+	Z
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	0	0

OR

	A	B	A^+B^+ X=0	A^+B^+ X=1	Z X=0	Z X=1
S_0	0	0	00	01	0	1
S_1	0	1	01	10	1	0
S_2	1	0	10	00	0	1
S_3	1	1	10	00	0	0

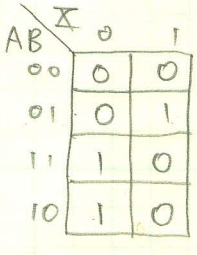
a) It is a Mealy network. ✓

b)

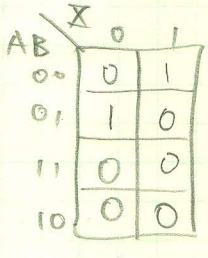


✓

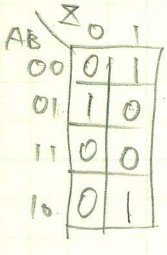
c)



D_a

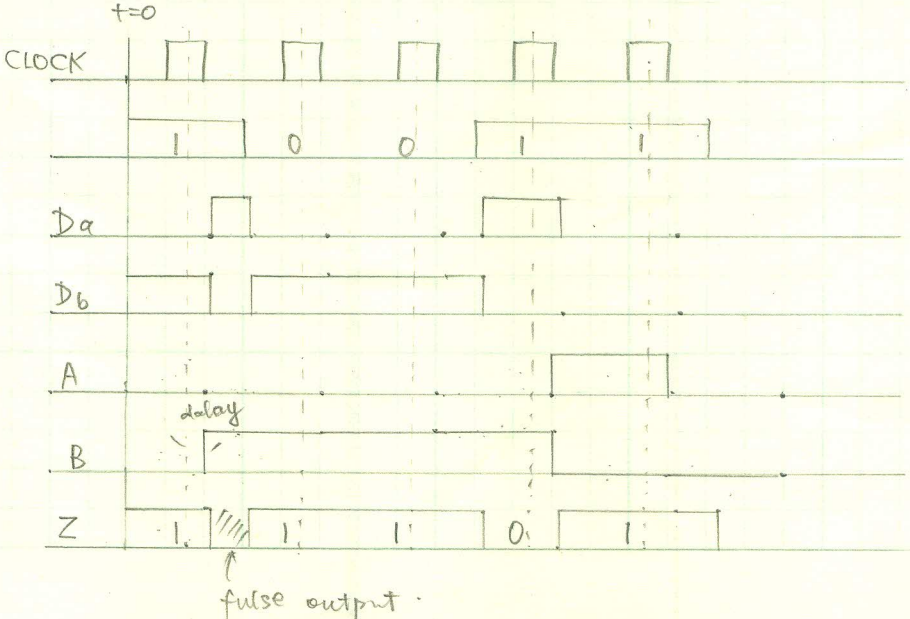


D_b



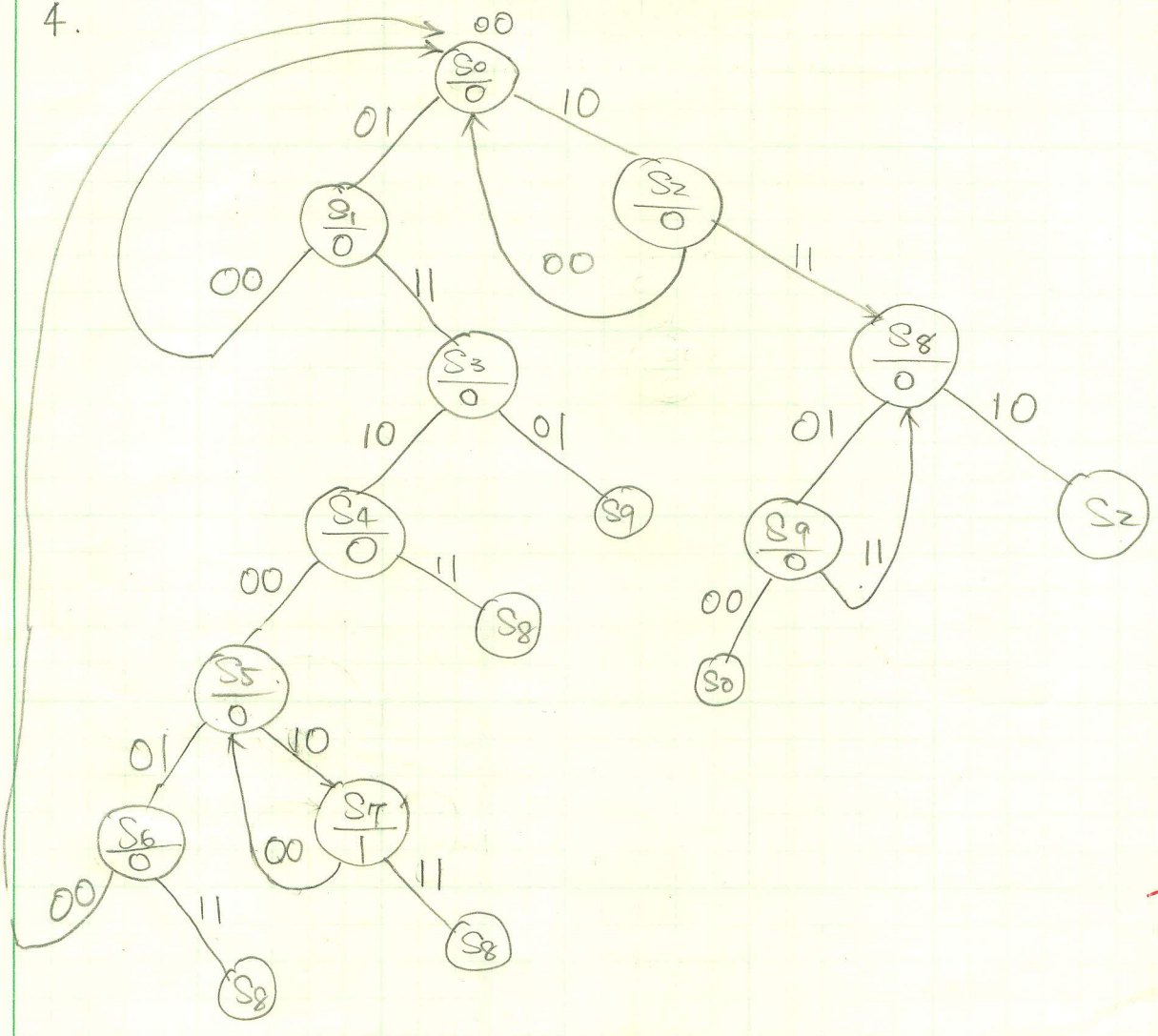
Z

$D_a = A\bar{X} + \bar{A}BX$ $\quad D_b = \bar{A}B\bar{X} + \bar{A}\bar{B}X$ $\quad Z = \bar{A}B\bar{X} + \bar{B}X$



✓

4.



-5

	00	01	11	10	Z
S0	(S0)	S1	—	S2	0
S1	S0	(S1)	S3	—	0
S2	S0	—	S8	(S2)	0
S3	—	S9	(S3)	S4	0
S4	S5	—	S8	(S4)	0
S5	(S5)	S6	—	S7	0
S6	S0	(S6)	S8	—	0
S7	S5	—	S8	(S7)	1
S8	—	S9	(S8)	S2	0
S9	S0	(S9)	S8	—	0

Six states are sufficient

Reducing : $S_0 \leftrightarrow S_5$

$S_1 \leftrightarrow S_6 \leftrightarrow S_9$

$S_3 \leftrightarrow S_8$

$S_2 \leftrightarrow S_4$

S_0, S_5	S_1-S_6, S_2-S_7	X
S_1, S_6	S_3-S_8	X
S_1, S_9	S_3-S_8	X
S_6, S_9	✓	
S_3, S_8	S_4-S_2	X
S_2, S_4	S_0-S_5	X

Reduced table

	00	01	11	10	Z 00	01	11	10
× S_0	(S0)	S_1	–	S_2	0	–	–	–
× S_1	S_0	(S1)	S_3	–	–	0	–	–
× S_2	S_0	–	S_8	(S2)	–	–	–	0
S_3	–	S_6	(S3)	S_4	–	–	0	–
S_4	S_5	–	S_8	(S4)	–	–	–	0
× S_5	(S5)	S_6	–	S_7	0	–	–	–
× S_6	S_0	(S6)	S_8	–	–	0	–	–
× S_7	S_5	–	S_8	(S7)	–	–	–	1
S_8	–	S_6	(S8)	S_2	–	–	0	–

Mealy merged :

	00	01	11	10	Z 00	01	11	10
(S_0, S_1)	(S0)	(S1)	S_3	S_2	0	0	–	–
(S_2, S_6)	S_0	(S6)	S_8	(S2)	–	0	–	0
S_3	–	S_6	(S3)	S_4	–	–	0	–
S_4	S_5	–	S_8	(S4)	–	–	–	0
(S_5, S_7)	(S5)	S_6	S_8	(S7)	0	–	–	1
S_8	–	S_6	(S8)	S_2	–	–	0	–

5. col 00 : $d \to a$, $f \to b$

01 : $a, g \to c$, $b, e \to d$

11 : $b \to a$, $f, c \to e$, $d \to g$

10 : $a, c, e \to b$, $g \to f$

$(a, d)_x$, $(b, f)_x$, $(a, g, c)_x$ $(b, d, e)_x$

$(a, b)_x$ $(f, c, e)_x$ $(d, g)_x$ $(a, b, c, e)_x$, $(f, g)_x$

a	d
b	e
f	c
α	g

Assignment :

a = 000
b = 001
c = 111
d = 001
e = 011
f = 110
g = 101
α = 100

	00	01	11	10	00	01	11	10
a	ⓐ	α	ⓐ	b	01	10	10	00
b	ⓑ	e	a	ⓑ	01	11	10	00
c	ⓒ	ⓒ	e	e	11	10	00	00
d	a	ⓓ	g	-	01	11	01	--
e	-	d	ⓔ	b	--	11	00	00
f	b	-	c	ⓕ	01	-	00	11
g	-	c	ⓖ	α	--	10	01	11
α	-	g	-	f	--	10	--	11