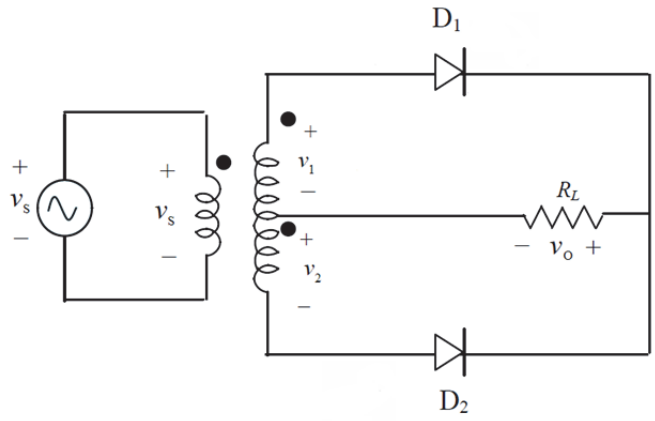
1. The rectifier supply shown in the figure below is used as part of an electronic device. The input is an AC voltage source with a frequency of 50 Hz and a peak amplitude of 200 V. The transformer primary to secondary ratio = 2:1. The load resistance is 100 Ω.

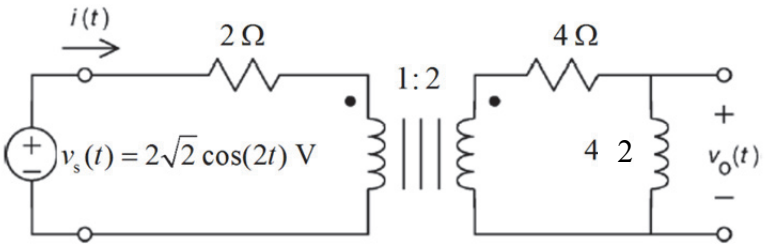


   (a) Determine the output DC voltage. What is the peak-to-peak ripple in the output voltage? What is the percentage ripple?

   (b) Sketch waveforms for v_s and v_o, respectively.

   (c) Suggest an additional component to be added to the above circuit, which can yield a smoother the output voltage. Draw the revised circuit.

2. Consider the transformer circuit shown in the figure below. The transformer turns ratio is 1:2. The input to the circuit is the voltage source, $v_s(t)$. Determine the output voltage, $v_o(t)$, across the 2 H inductor.



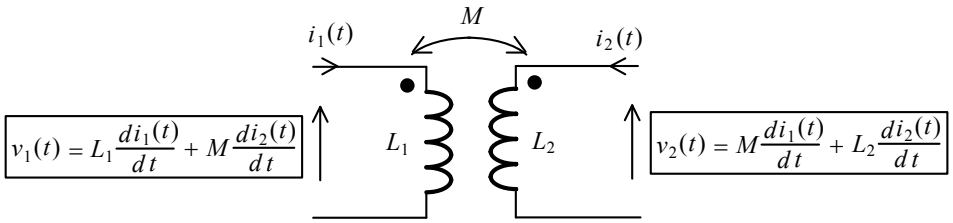
3. A DC power supply consists of a transformer feeding a half-wave rectifier together with a capacitor filter. It supplies a DC current of 1 A at 20 V DC to an electronic equipment. The AC input source is 230 V (rms) at 50 Hz. The filter capacitor has a capacitance of 60,000μF.

   a) Draw the circuit diagram of the supply arrangement.

   b) Determine a suitable winding ratio for the transformer.

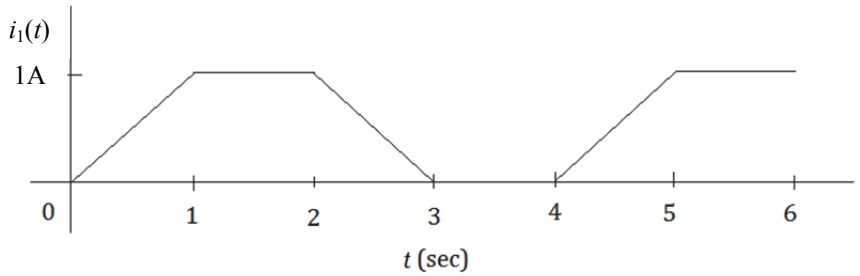
   c) Determine the magnitude of the peak-to-peak ripple in the output voltage.

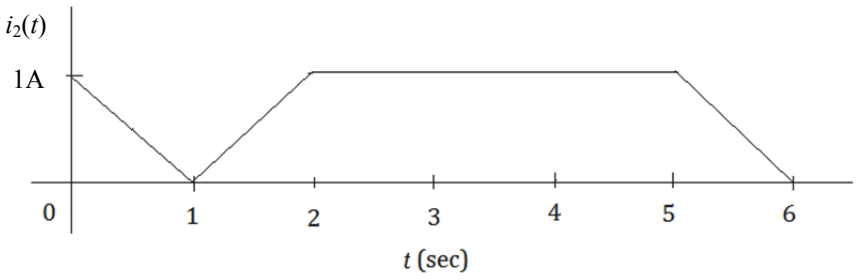
4. Shown in the figure below are the expressions of the primary and secondary voltages of an ideal transformer. Assume that the transformer reluctance $\Re = 25$, the numbers of the turns of the primary and secondary windings are $N_1 = 10,\ N_2 = 5$, respectively.



$L_1 = \frac{N_1^2}{\Re},\ L_2 = \frac{N_2^2}{\Re},\ M^2 = L_1 L_2$ for no flux leakage and perfect coupling

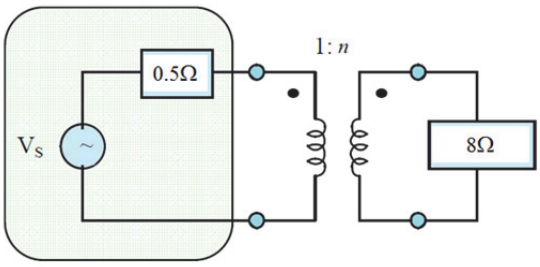
(a) Given the waveforms of $i_1(t)$ and $i_2(t)$ as the figure below,





sketch the waveforms of the induced voltages, $v_1(t)$ and $v_2(t)$.

5. A sound system with a loudspeaker can be represented in a circuit diagram below. Assume that the internal resistance of the source is 0.5Ω, and the resistance of the load is 8 Ω.



(a) Find an appropriate transformer turns ratio, which results in impedance matching.

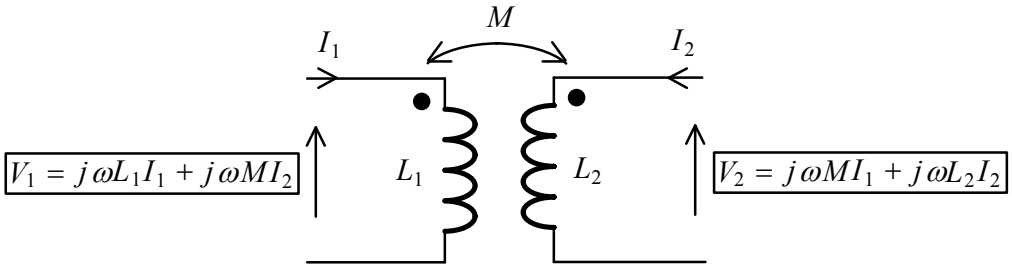
(b) Given $v_s(t) = 230\sqrt{2}\cos(\omega t)$ V and with the transformer turning ratio obtained in (a), find the average powers consumed by the load and by the internal resistor.

(c) Given $v_s(t) = 230$ V and again with the transformer turning ratio obtained in (a), find the actual powers consumed by the load and by the internal resistor.

(d) For both (b) and (c), determine the power consumed by the transformer.

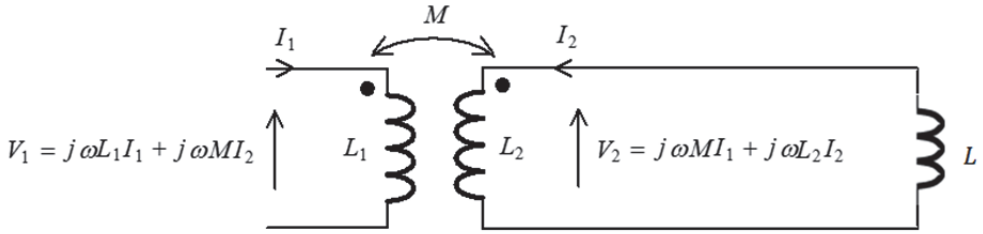
6. Suggest a DC power supply circuit that can be used to step down the electric source from the mains (230V AC) to power up your laptop, which takes 5V DC. Draw the circuit with necessary components. Will you use your design for your own laptop? Why or why not?

7. For AC environments, show that the primary and secondary voltages in the phasor form are given as those in the figure below.



Hint: Assume $i_1(t) = \sqrt{2}\, r_1 \cos(\omega t + \theta_1)$ and $i_2(t) = \sqrt{2}\, r_2 \cos(\omega t + \theta_2)$.

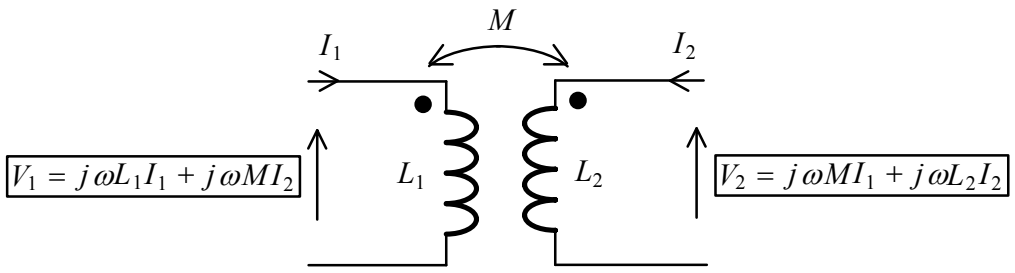
8. The transformer is connected to a load inductor with inductance L = 2 H, as shown in the figure below. Recall that the transformer reluctance $\Re = 25$, the numbers of the turns of the primary and secondary windings are $N_1 = 10,\ N_2 = 5$, respectively. Determine the ratio of the primary and secondary currents (in phasor).



Why is the usual transformer property below no longer valid in such a situation?

$$\frac{I_1}{I_2} = -\frac{N_2}{N_1}$$

9 Shown in the figure below are the expressions of the primary and secondary voltages of an ideal transformer in the phasor form in AC environments.



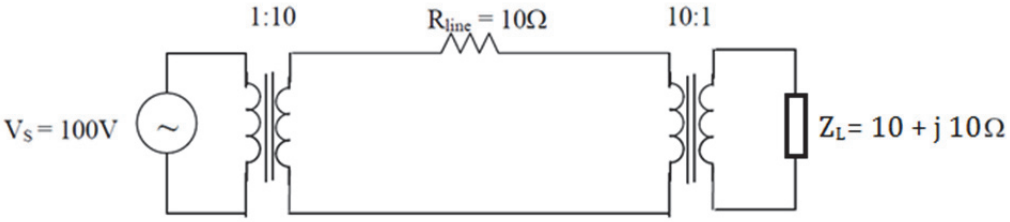
The primary and secondary inductances of the transformer are respectively given by

$$L_1 = \frac{N_1^2}{\Re}, \quad L_2 = \frac{N_2^2}{\Re}, \quad M = \sqrt{L_1 L_2}$$

where $\Re$ is the reluctance of the transformer. Let $V_{1,\text{peak}}$ and $V_{2,\text{peak}}$ are respectively the peak values of the primary and secondary voltages of the transformer. Show that

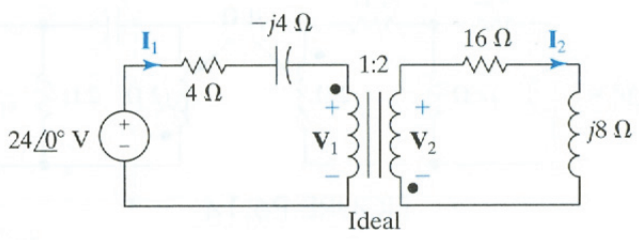
$$\frac{V_{2,\text{peak}}}{V_{1,\text{peak}}} = \frac{N_2}{N_1}$$

10. The following transmission system is used to transmit electric power from the source to an AC device.

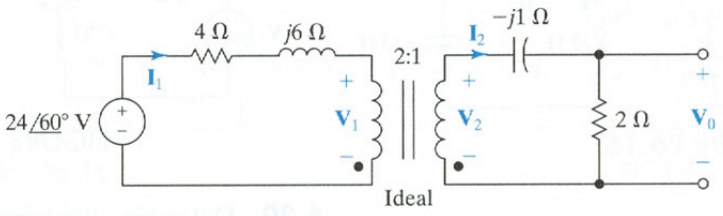


Determine the average power lost on the transmission line and the average power consumed by the load. What is the power efficiency?

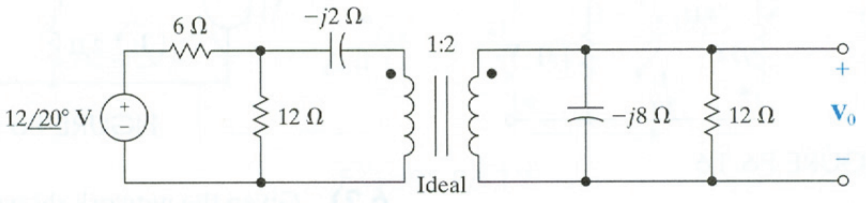
11. Find I_1 and I_2 in the circuit below.



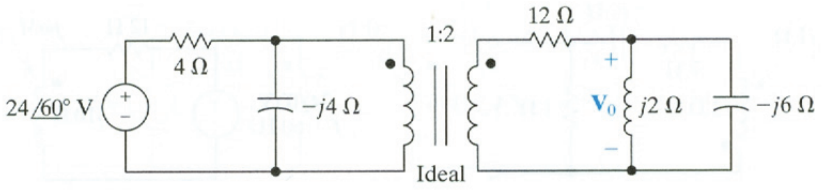
12. Find all voltages and currents in the circuit below.



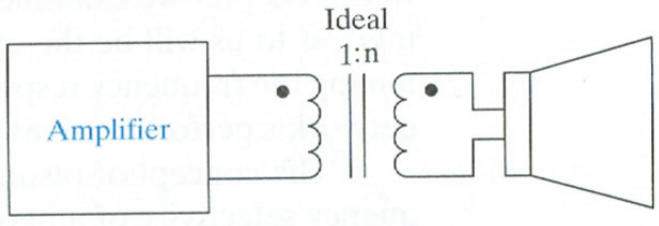
13. Find V_0 in the circuit below.



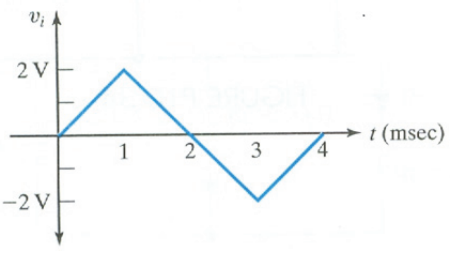
14. Find V_0 in the circuit below.

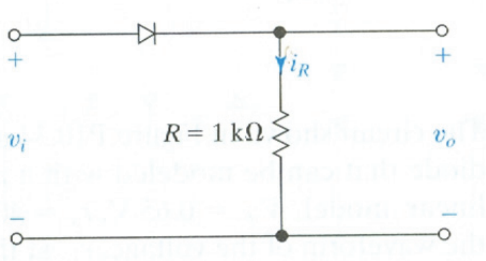


15. The output stage of an amplifier is to be matched to the impedance of a speaker as show in the figure below. If the impedance of the speaker is 8 Ω and the amplifier requires a load impedance of 3.2 kΩ, determine the turns ratio of the ideal transformer.

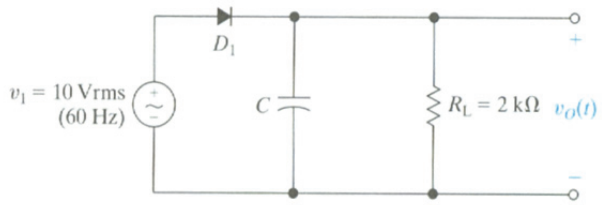


16. The waveform shown below is applied as an input to the half-wave rectifier circuit below. (a) Plot the output waveform, $v_o(t)$. (b) What is the dc voltage output?



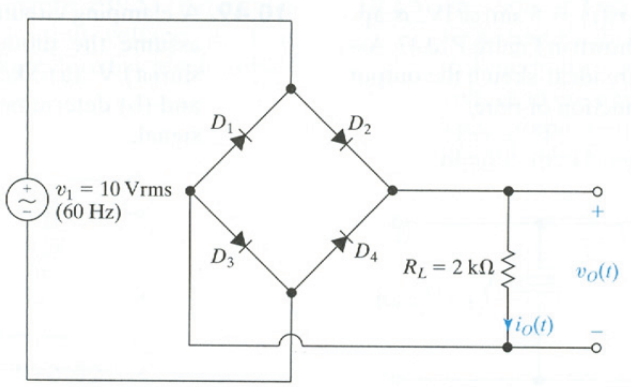


17. Shown below is a half-wave rectifier circuit with a filter. Plot the output waveform and estimate the peak-to-peak ripple for C = 150 μF.

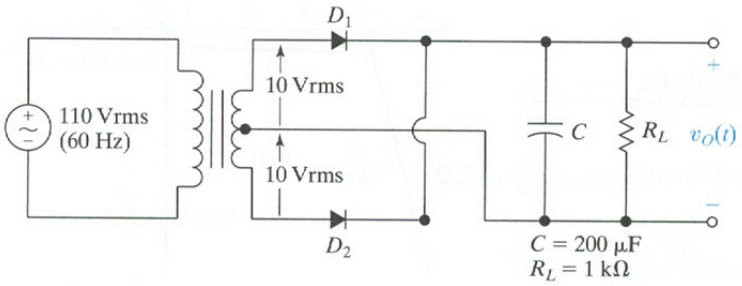


18. An electronic calculator operates on a dc supply of 6 V. This supply is obtained from a half-wave rectifier with a filter. If the calculator can be modeled as a 10 kΩ resistance and it can tolerate a maximum peak-to-peak variation of 0.1 V around the dc value, calculate the minimum value of capacitor that can be used in the filter. Assume ac input is 50 Hz.

19. Shown below is a four-diode full-wave rectifier circuit. (a) Plot the output voltage $v_o(t)$. (b) Determine the maximum reverse voltage on any diode. (c) What is the dc output voltage?



20. Shown below is a two-diode full-wave rectifier circuit. Plot the output voltage waveform, and estimate the peak-to-peak ripple. Determine the maximum reverse voltage on either diode.



21. A majority detector has three input variables **A**, **B** and **C** and two output light indicators. Green light (**G**) will be on if majority of the input variables are equal to 1. Red light (**R**) will be on if majority of the input variables are equal to 0.

    (a) Construct a truth table for your design.

    (b) Obtain logical expressions for **G** and **R**, respectively.

    (c) Draw logic circuit implementations for **G** and **R**.

22. Prove the following De Morgan's law:

$$\overline{A+B+C} = \overline{A}\cdot\overline{B}\cdot\overline{C}$$

23. Use the De Morgan's laws and any of first 17 rules of Boolean Algebra to prove the last rule, i.e., Rule 18:

$$A+\overline{A}\cdot B = A+B$$

24. Consider a logical expression

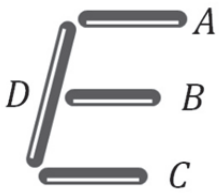
$$W = \overline{(A+\overline{C})}\cdot(B+C)$$

a) Construct a truth table for *W*.

b) Use the Karnaugh map technique to simply the logical expression.

c) Implement the logical expression obtained in (ii) using only 2 two-input NOR gates.

25. An LED display panel shown in the figure below has four LED light bars labeled ***A***, ***B***, ***C*** and ***D***, respectively. You are required to design an appropriate digital logic circuit to display Letters ***F*** and ***L*** using the panel.



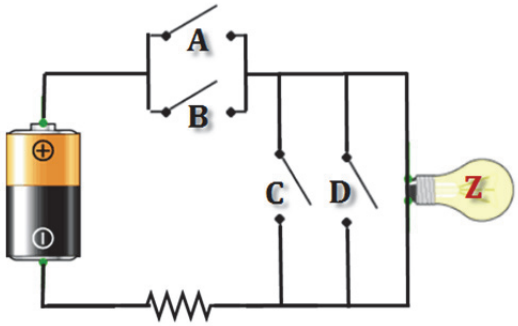
(a) Construct a truth table for your design.

(b) Obtain logical expressions for ***F*** and ***L***, respectively.

(c) Draw logic circuit implementations for ***F*** and ***L*** using only 2-input NOR gates (i.e., each NOR gate only has two input channels). For each letter, you cannot use more than 8 NOR gates for the implementation.

(d) What other English letters can be displayed by the panel?

26. Derive a logical expression for the switch circuit shown in figure below.



27. The truth table below shows the relationship between inputs **A, B, C** and **D**, and output **Z**.

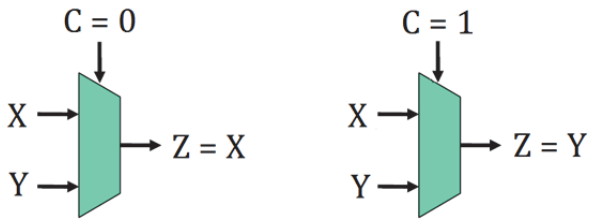
(a) Find **Z** in terms of **A, B, C** and **D** in the Sum-of-products (SOP) form.

(b) Simply the expression obtained using Karnaugh map.

(c) Implement the logical expression obtained in (b) using no more than 4 two-input NOR gates (i.e., each NOR gate only has two input channels).

A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

28. A multiplexer is a device setting its single output to the same value as one of its many inputs. Shown in the figure below is a multiplexer of two inputs, X and Y, in which X is selected when the control input C = 0 and Y is selected when C = 1.



(a) Assume that both X and Y are logical variables, construct a truth table for the above multiplexer.

(b) Obtain a logical expression for Z in the SOP form.

(c) Use Karnaugh map to simplify the expression of Z obtained in Part (b).

(d) Draw a logic circuit implementation for Z using no more than 7 two-input NOR gates (i.e., each NOR gate only has two input channels).

29. Prepare a truth table for each of the following Boolean expressions:

(a) $F = A \cdot \overline{B} + \overline{A} \cdot B$

(b) $F = A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C + A \cdot B \cdot C$

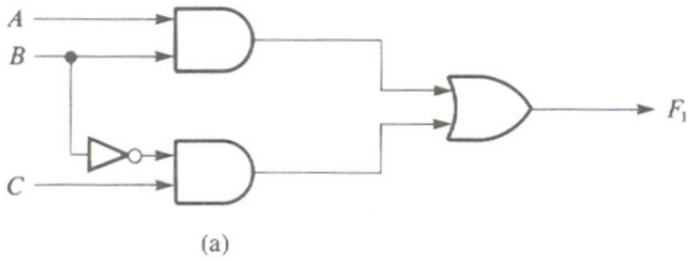
30. Without using K maps, simply the following Boolean expressions:

(a) $F = A \cdot C + C \cdot D + B \cdot C \cdot D$

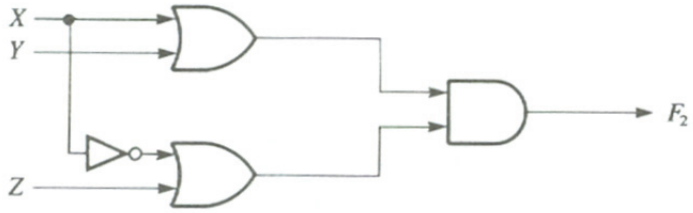
(b) $F = A \cdot B \cdot \overline{C} + B \cdot C + A \cdot B \cdot D + B \cdot C \cdot D$

31. Using K maps, simply the Boolean expressions in Problem 30.

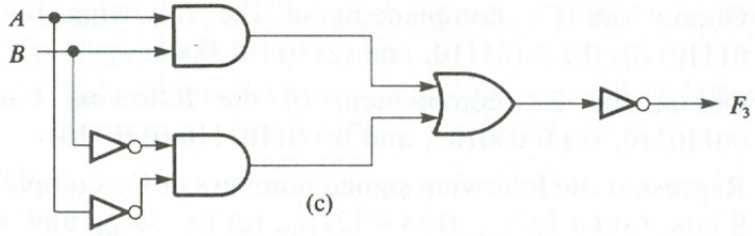
32. Derive the Boolean expressions for the logic circuits shown below.



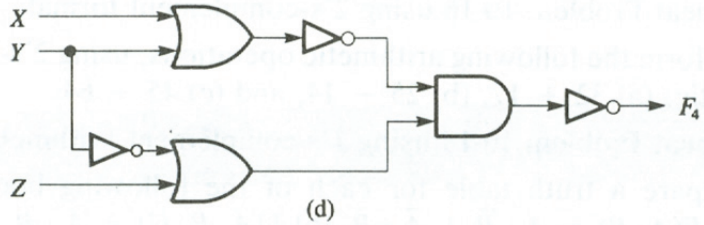
(a)



(b)



(c)



(d)

33. Draw the logic diagram for the following Boolean expressions, without simplifications:

(a) $F = A \cdot B + \overline{B} \cdot C + A \cdot B \cdot D + A \cdot C \cdot D$

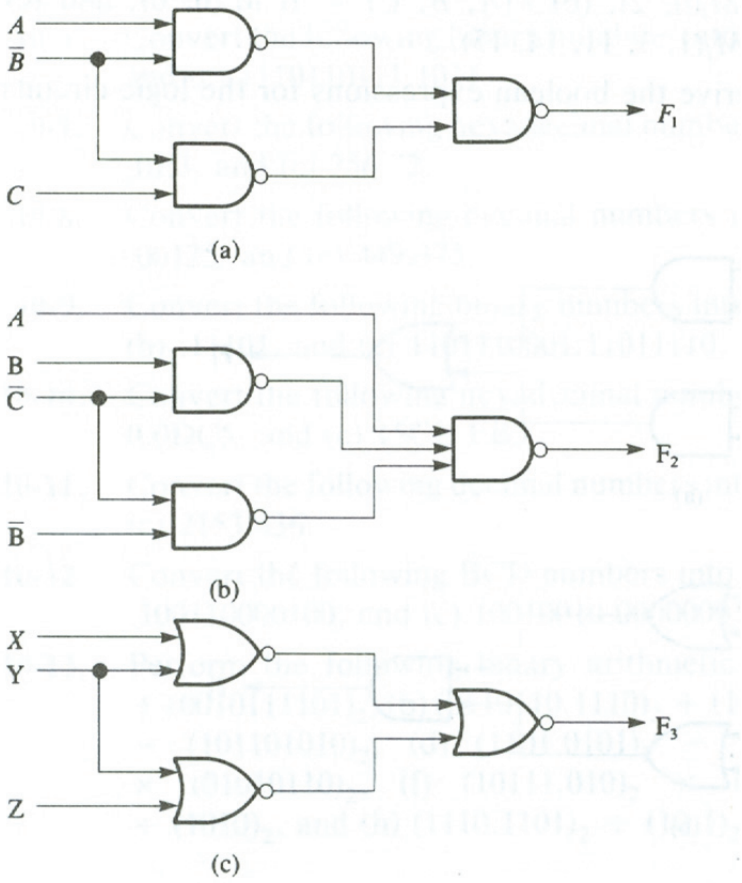
(b) $F = (X + Y) \cdot (\overline{X} + Z) \cdot (Y + \overline{Z})$

(c) $F = \overline{\overline{A \cdot C} + B \cdot \overline{C} + A \cdot B \cdot C}$

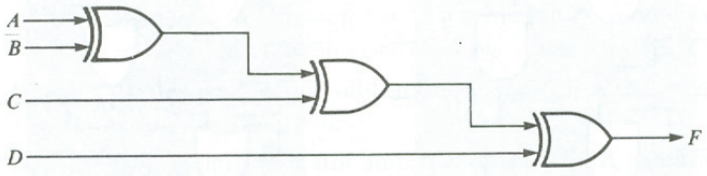
(d) $F = \overline{(X + Y) \cdot \overline{(X + \overline{Z})} \cdot (Y + Z)}$

34. Repeat Problem 33 with simplification.

35. Derive the Boolean expressions for the logic circuits below.



36. The logic circuit below is known as a parity checker for a 4-bit binary number. (a) Derive its Boolean expression. (b) Prepare its truth table. (c) Can you realize the same function by using fewer logic gates?



37. The logic circuit shown below is one part of the magnitude comparator used to compare two binary numbers. (a) Prepare its truth table. (b) Can you describe this circuit?